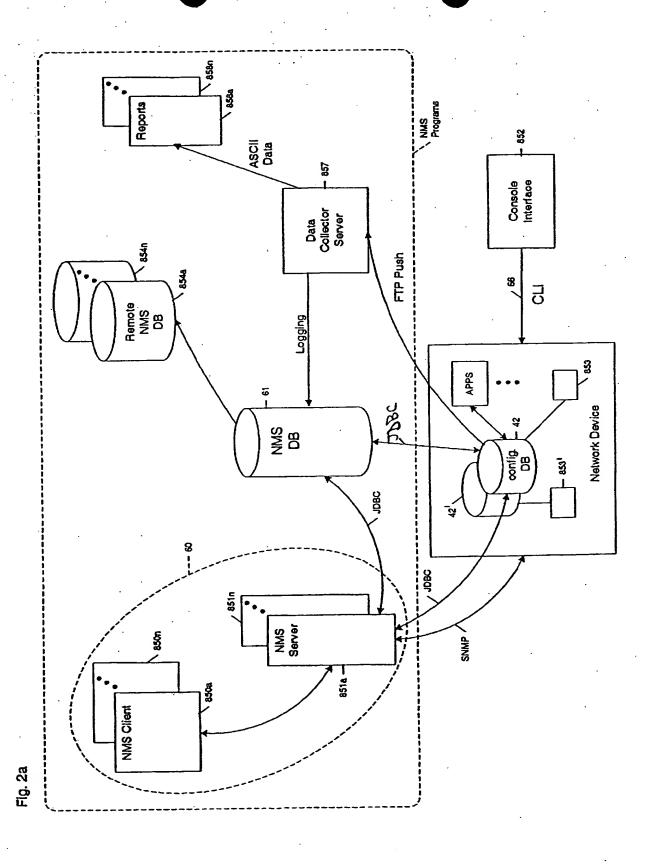
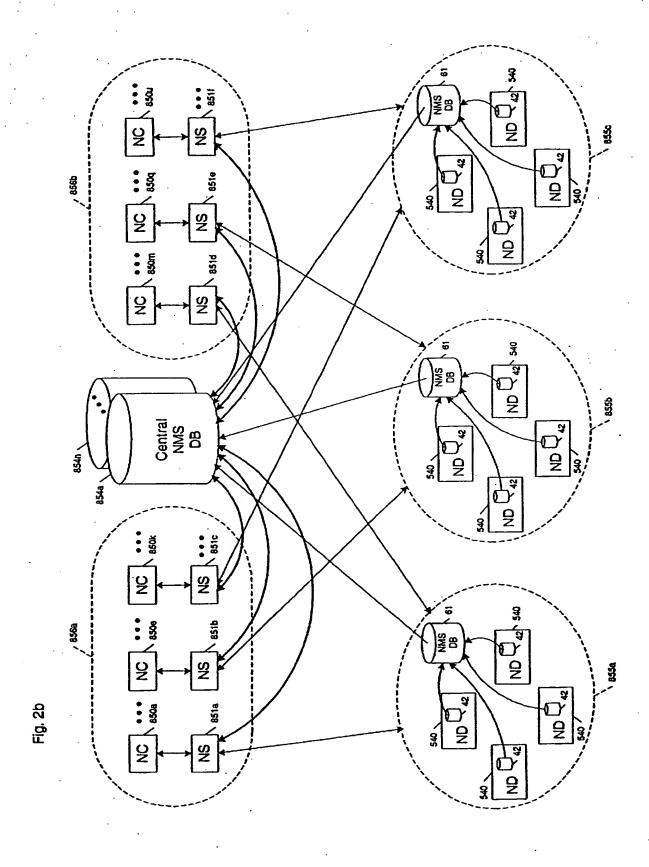
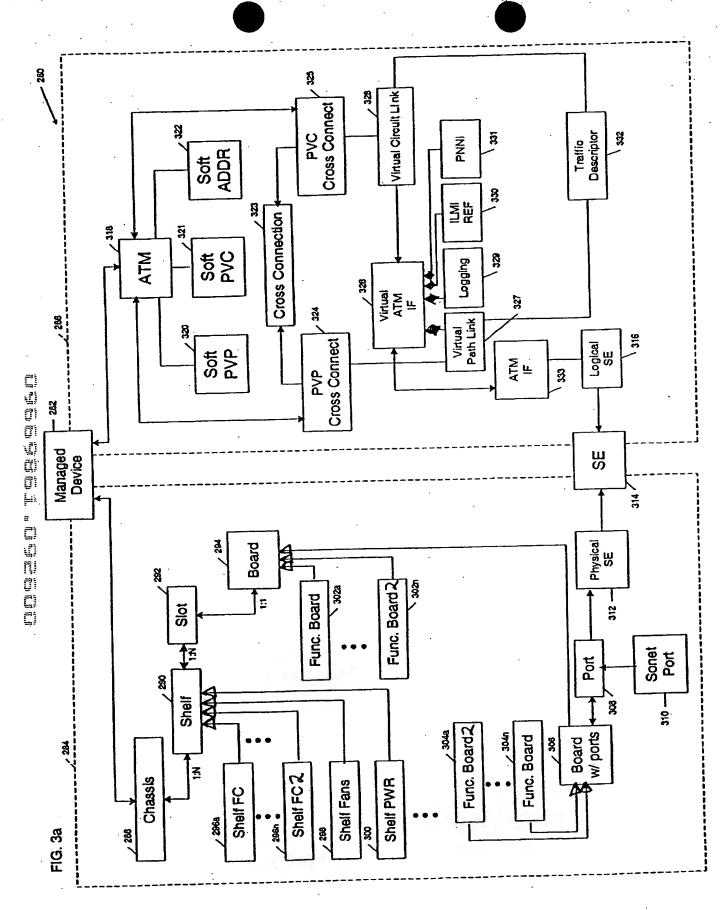
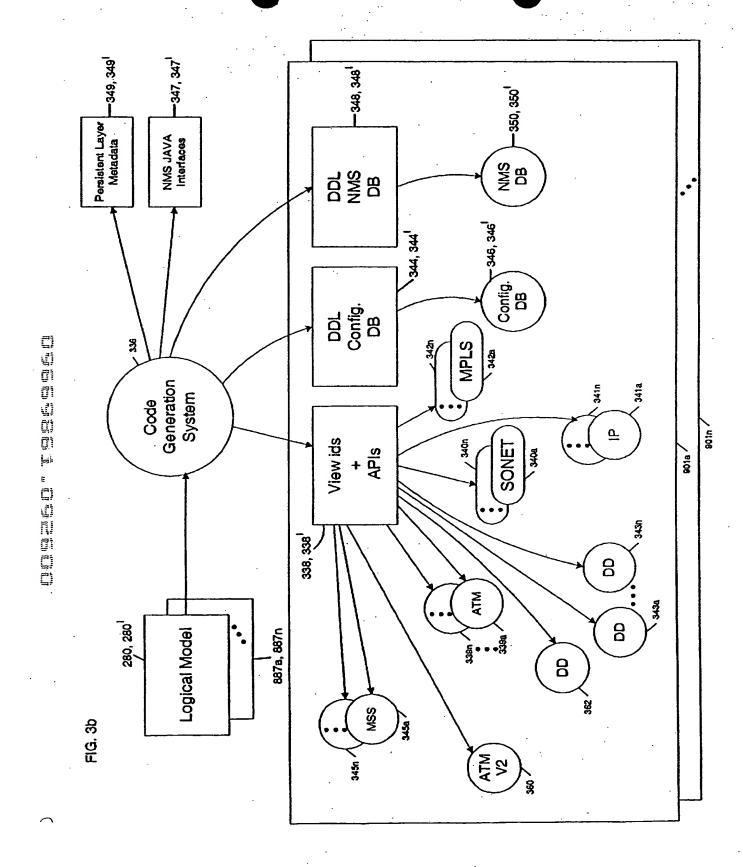


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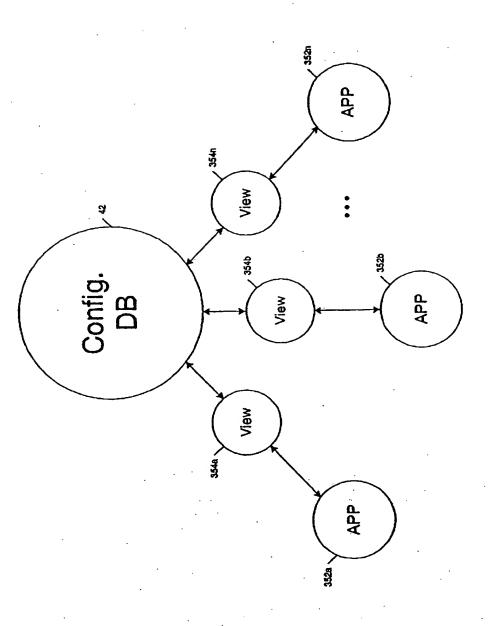
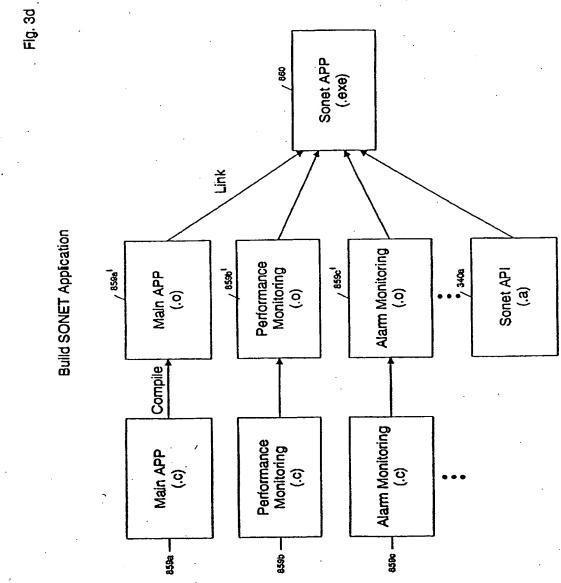
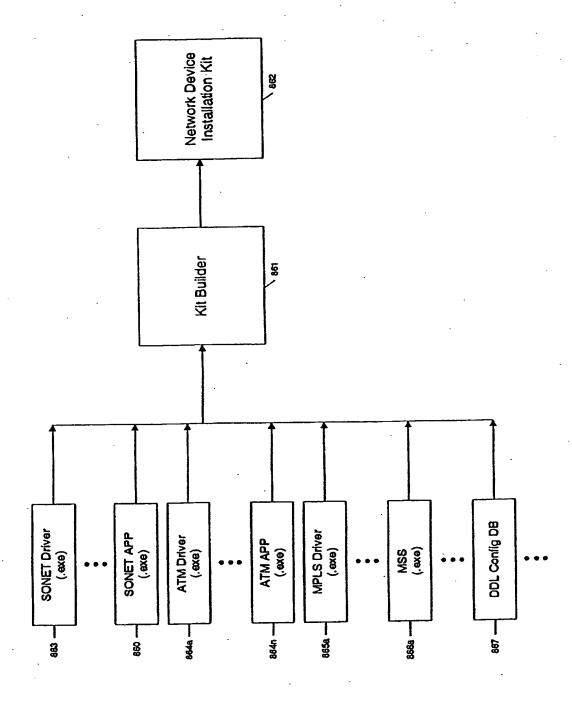


FIG. 30







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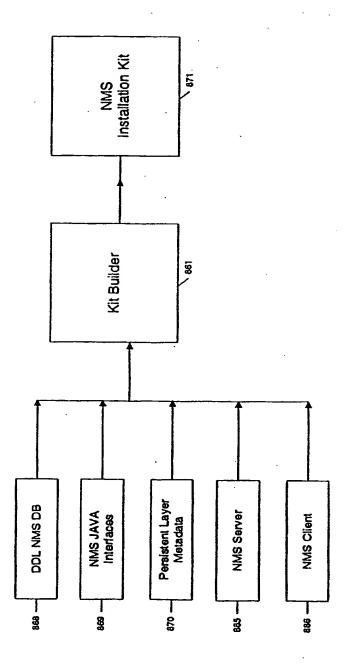
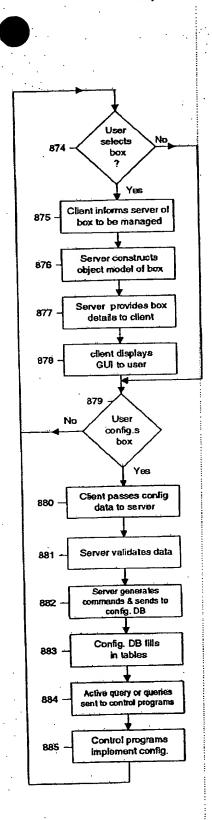


Fig. 35

Fig. 3g

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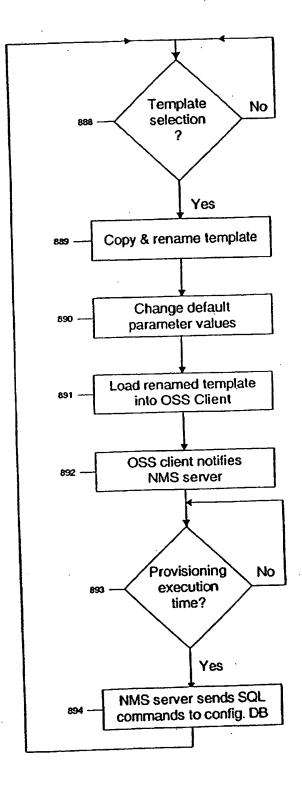
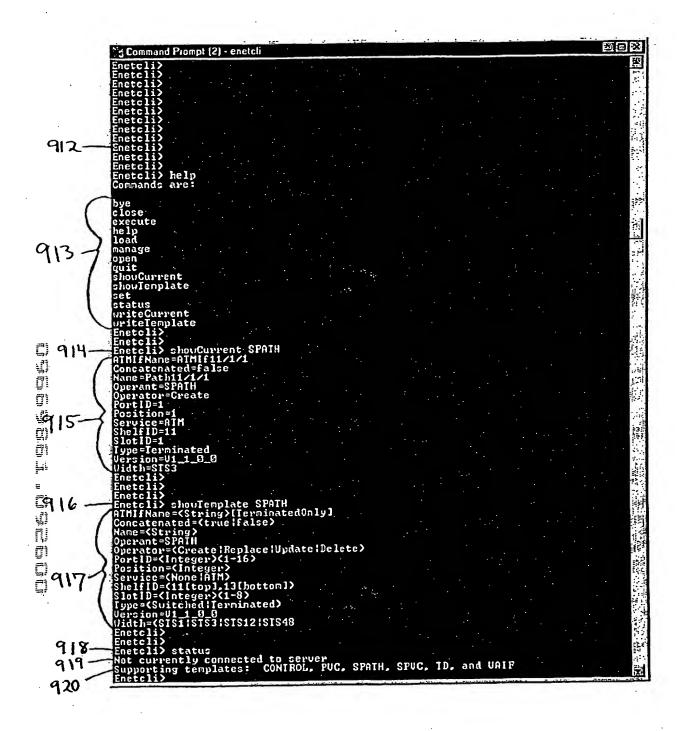


Fig. 3h



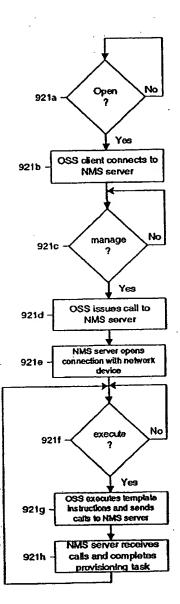
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Fig.3i

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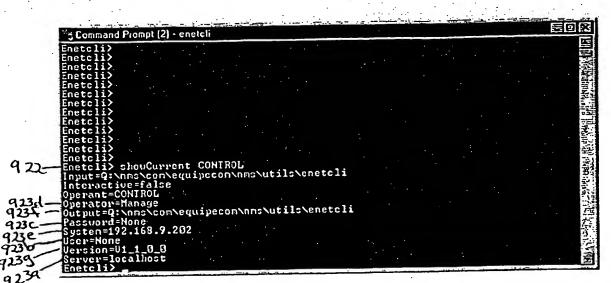
Fig. 3j



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Fig.3L

1924 BATCH.

Operant=BATCH
Operator=Execute
Version=V1_1_0_0

1249 — Task1=execute-SPATH
1246 — Task2=execute-PVC
1246 — Task3=execute-SPVC
1246 — Task4=load-SPVC-spvc1
1246 — Task6=load-SPVC-spvc2
1246 — Task6=load-SPVC-spvc2

9249—Task50=sct-SPATH-PortID-3 9241—Task51=execute-SPATH 9241—Task52=set-SPATH-SlotID-2 9241—Task53=execute-SPATH

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Fig.3M

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Operant=BATCH Operator=Execute - Version=V1_1_0_0 925a—Task1=execute-CONTROL 9255 -Task2=execute-SPATH 925C Task3=set-SPATH-PortID-3 925d Task4=execute-SPATH

Task61=set-CONTROL-System-192.168.9.201 Task62=execute-CONTROL -Task63=execute-SPATH

Task110=set-CONTROL-Server-Scrver1
Task110=set-CONTROL-System-192.168.8.200
Task111=execute-CONTROL
Task111=execute-CONTROL -Task112=execute-SPATH 4 G) (Ti

(1) (1) (1) (2) (2) (2) (2)



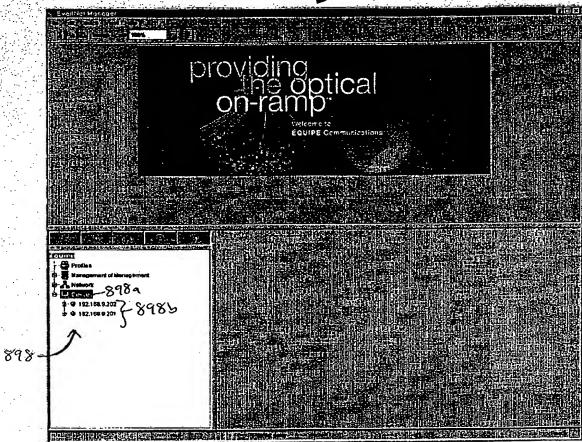


Fig.4a

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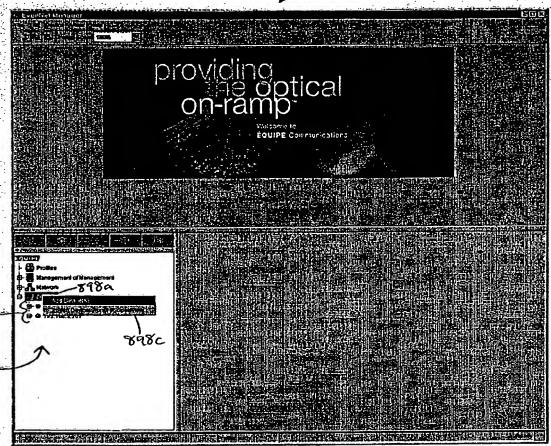


Fig.45



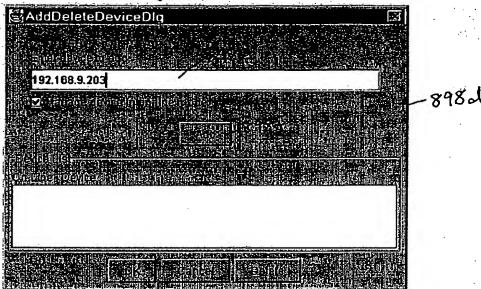
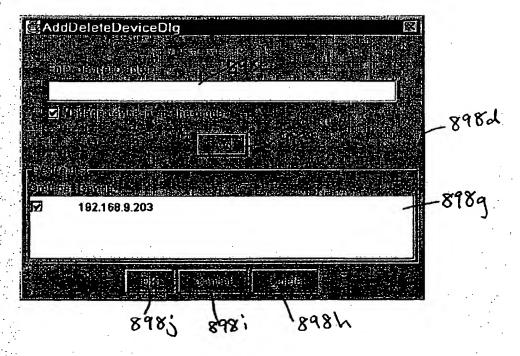


Fig. 4d



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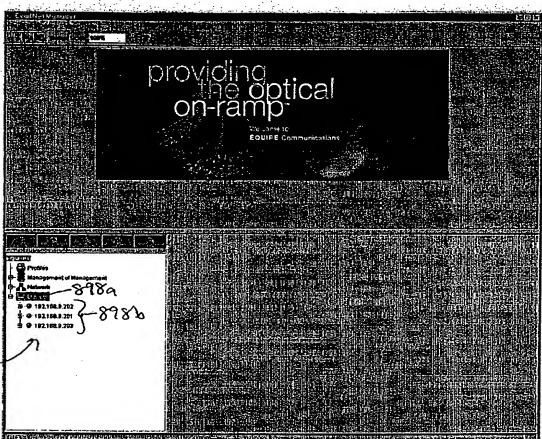
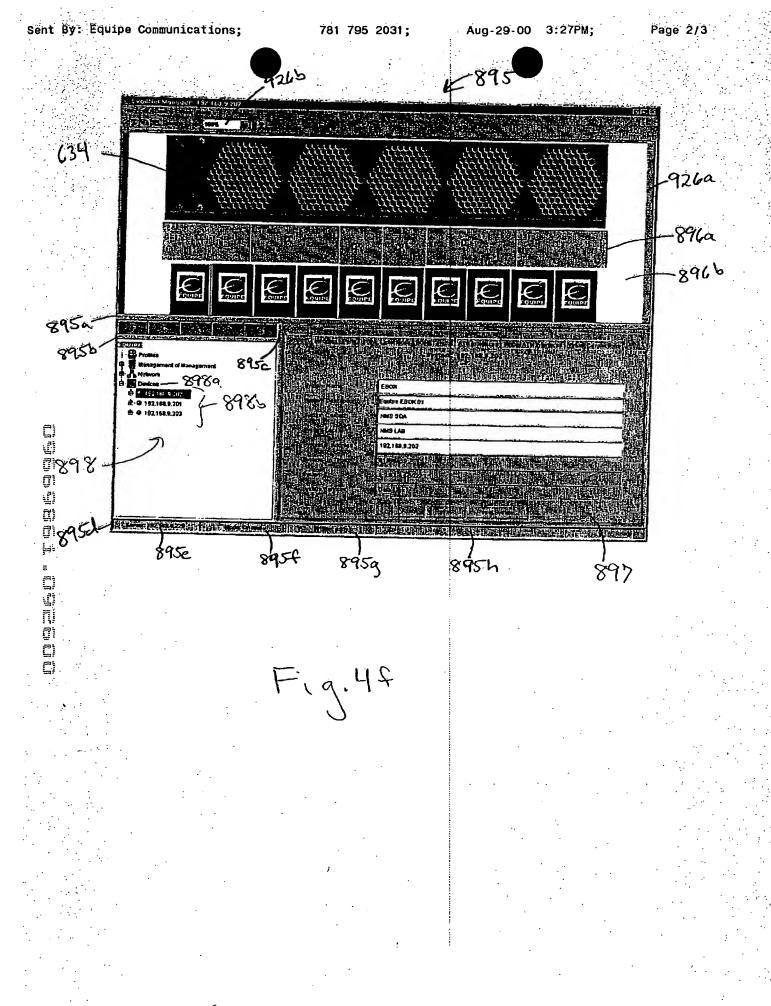


Fig.4e



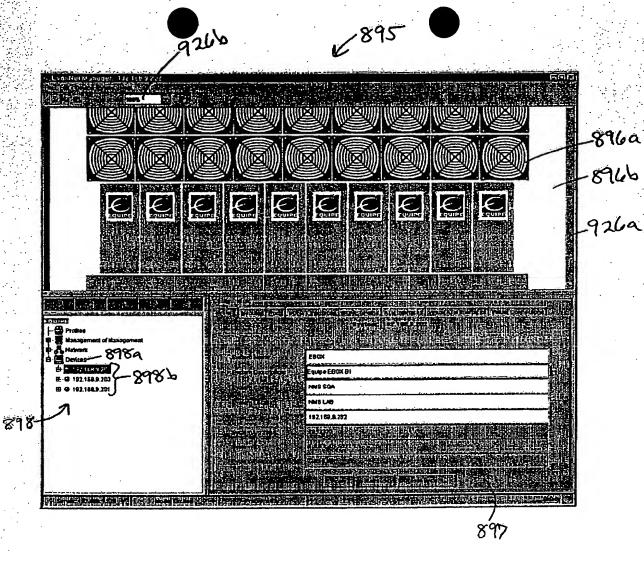


Fig.49

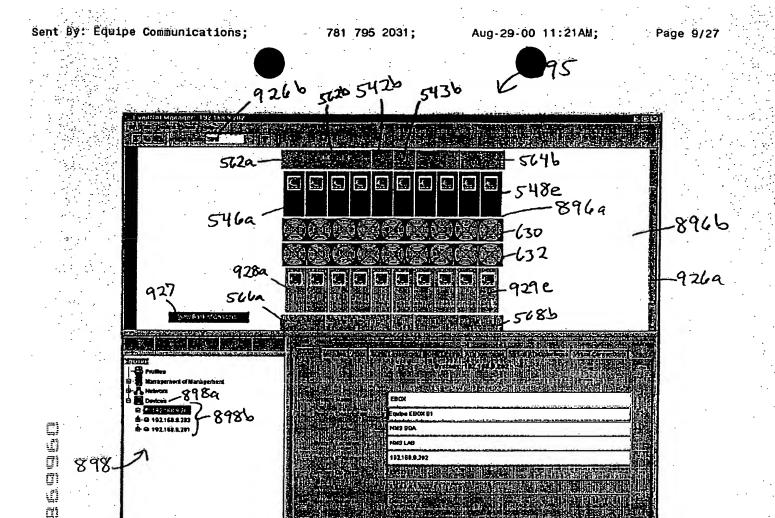
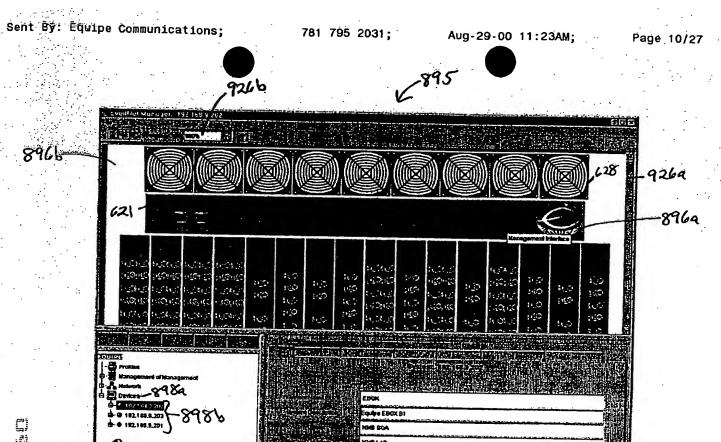
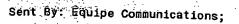


Fig. 4h

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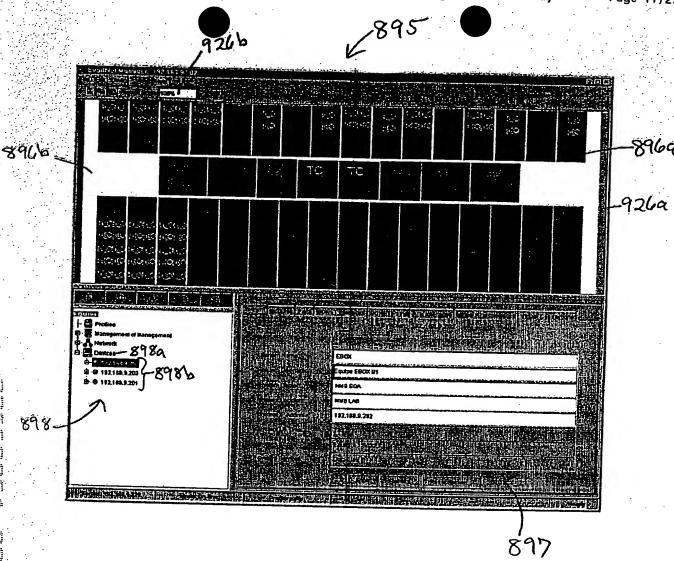


Fig. 4j

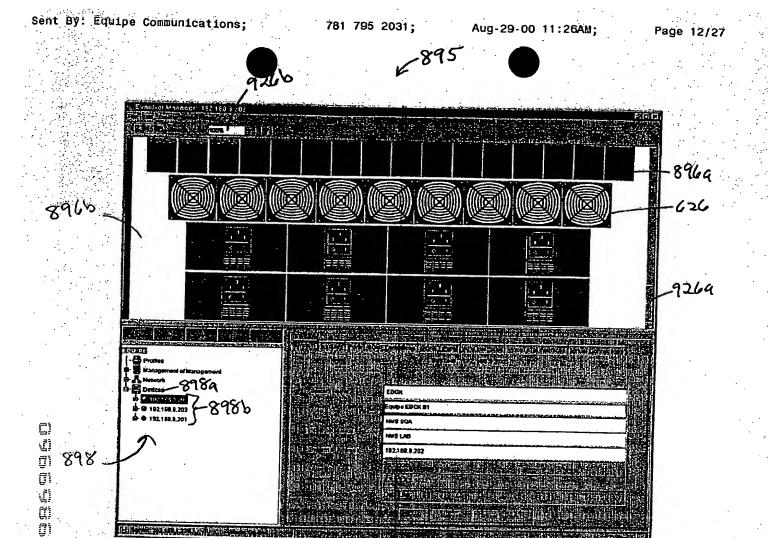


Fig.4K

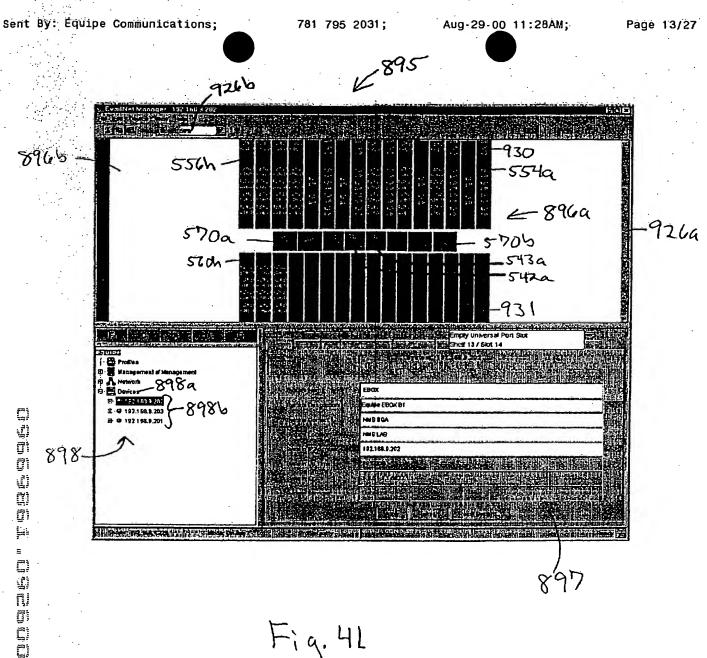


Fig. 4L

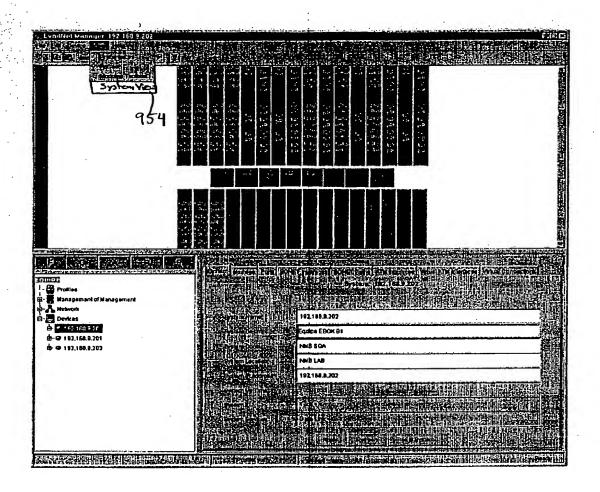


Fig. 4m



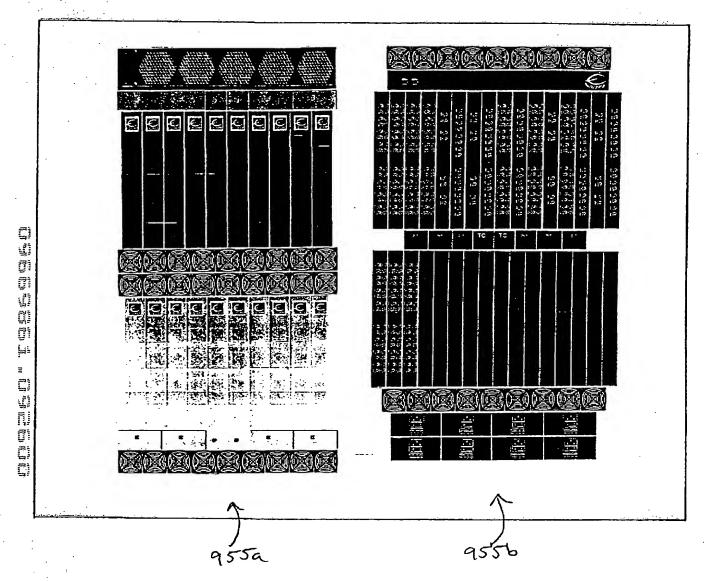


Fig.4n

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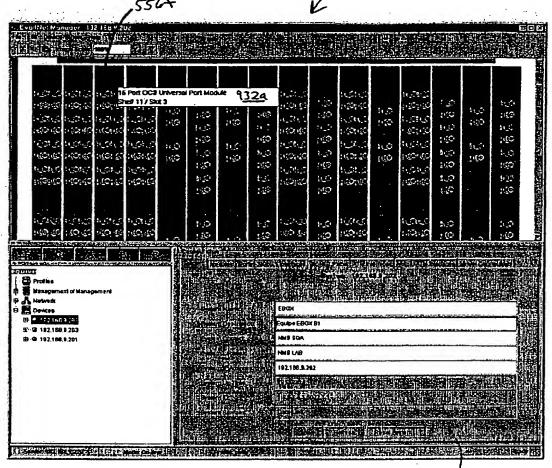
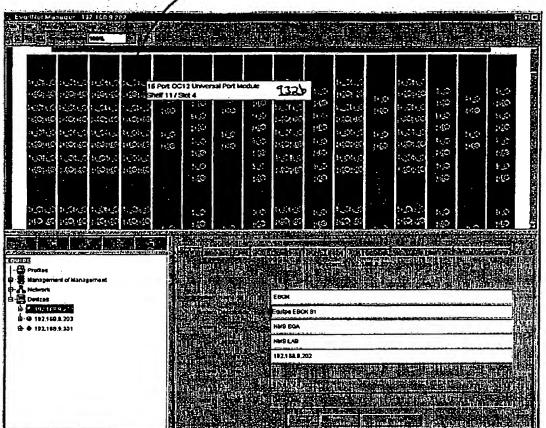


Fig.40

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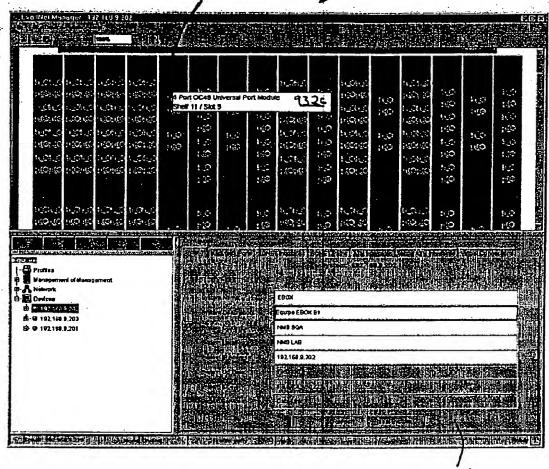
Fig.4P

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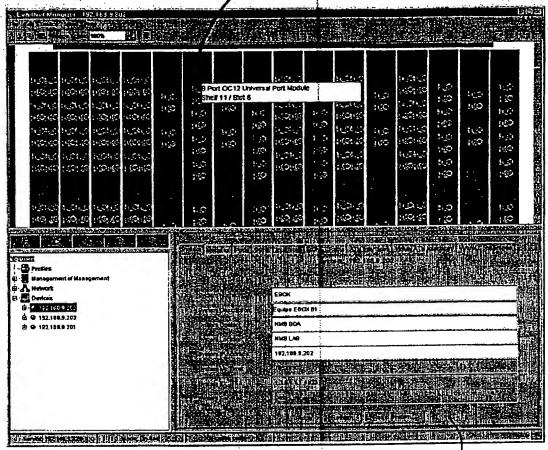
Fig. 48

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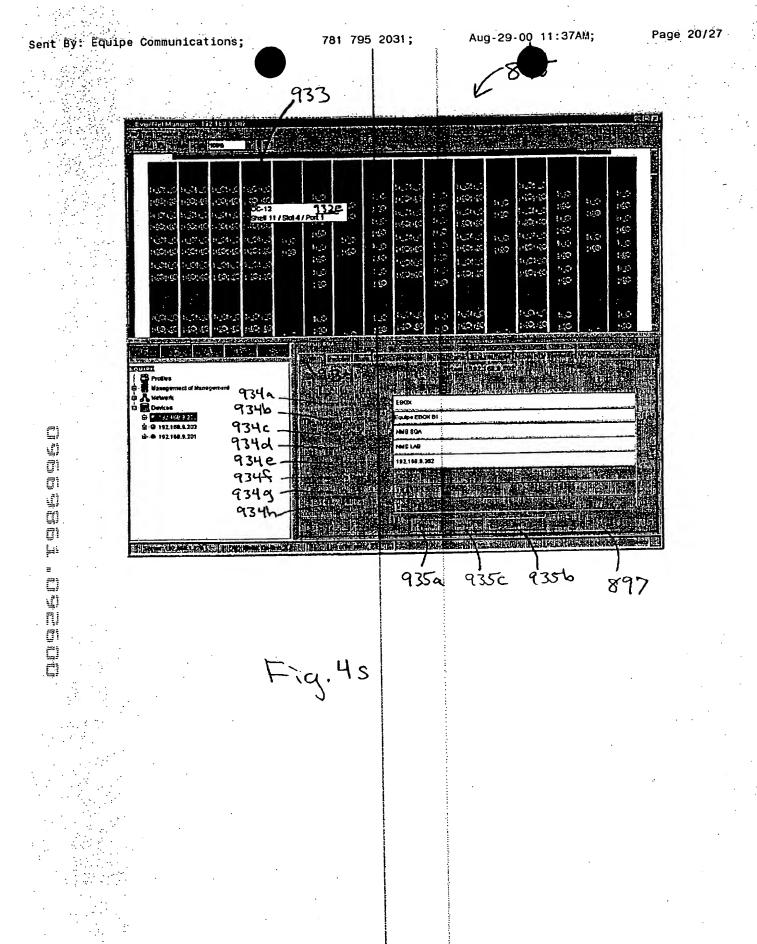
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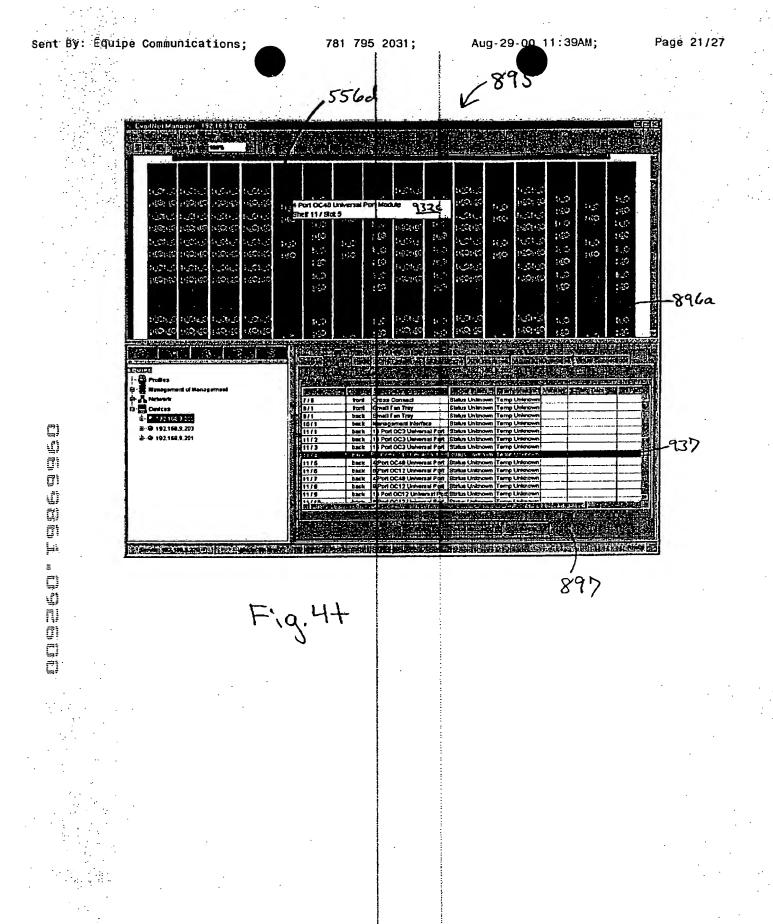
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Fig. 4-





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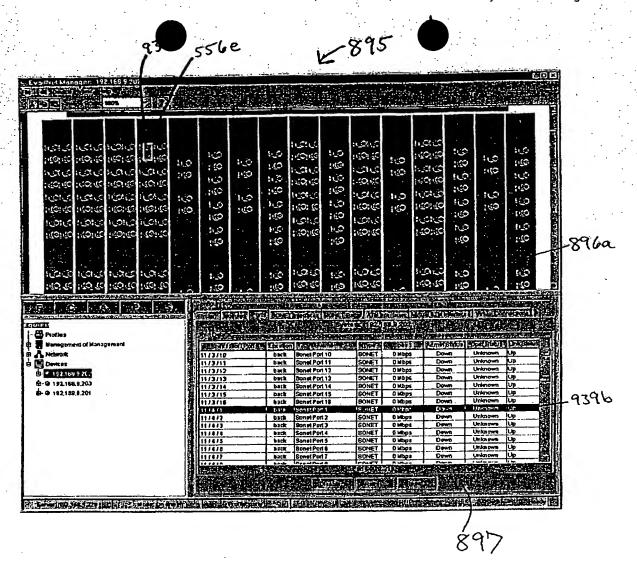
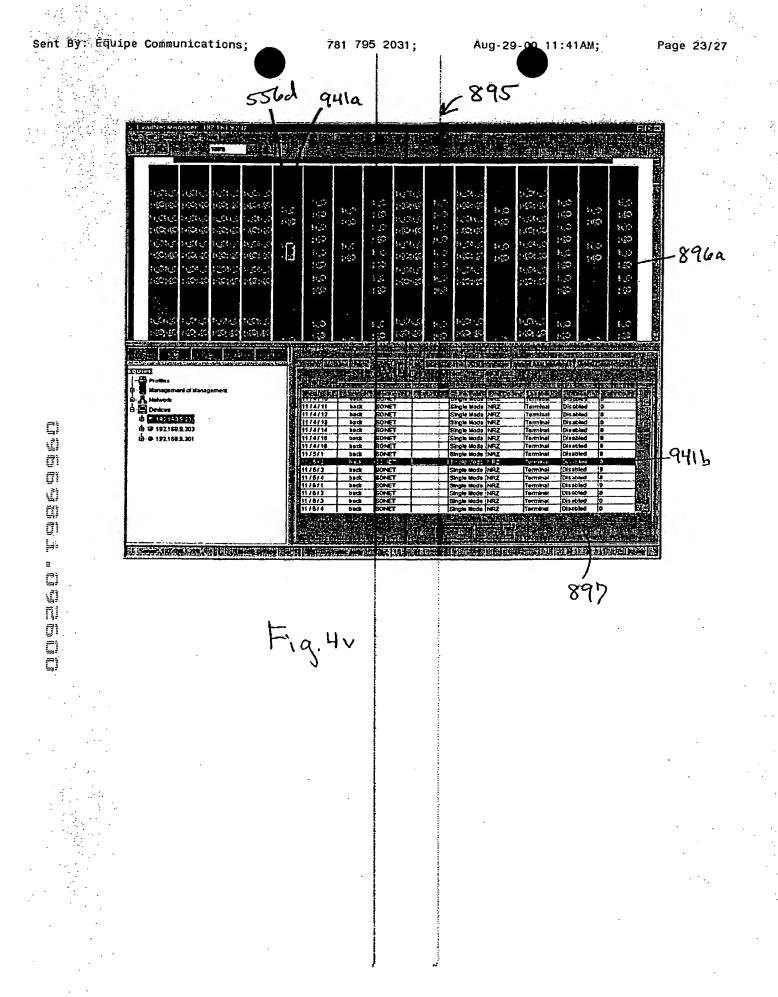
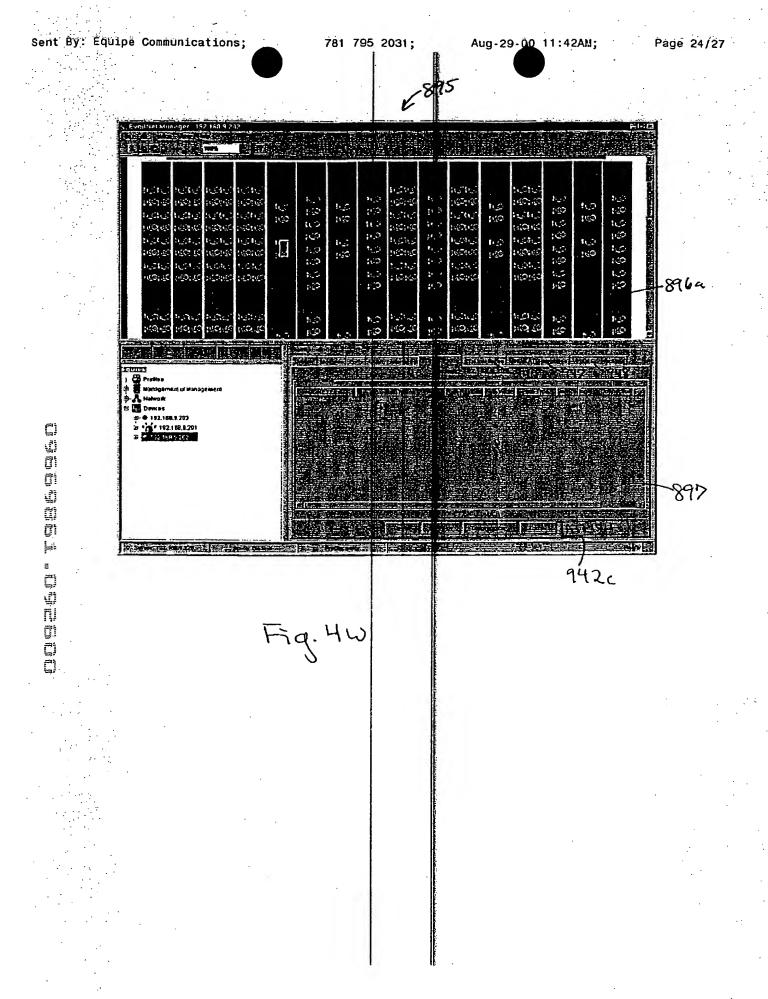
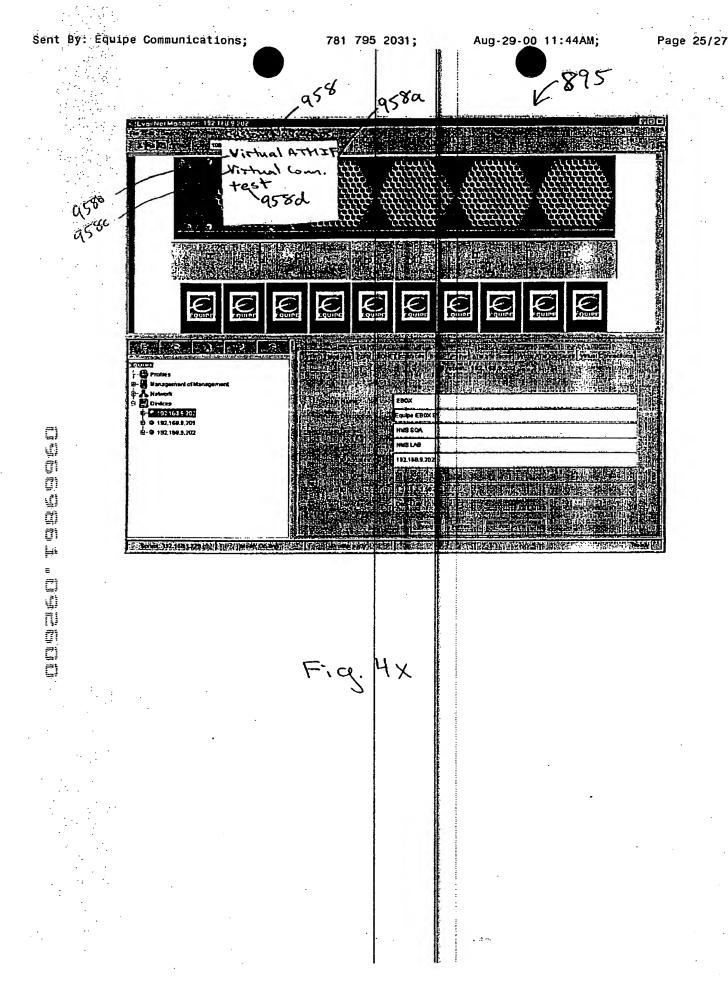
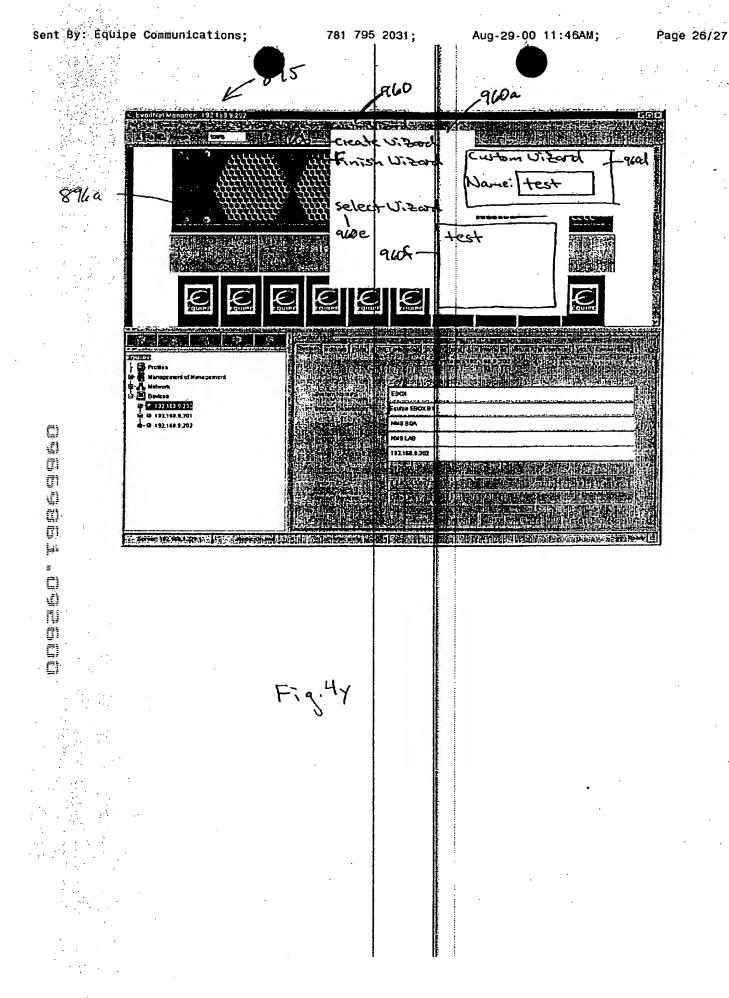


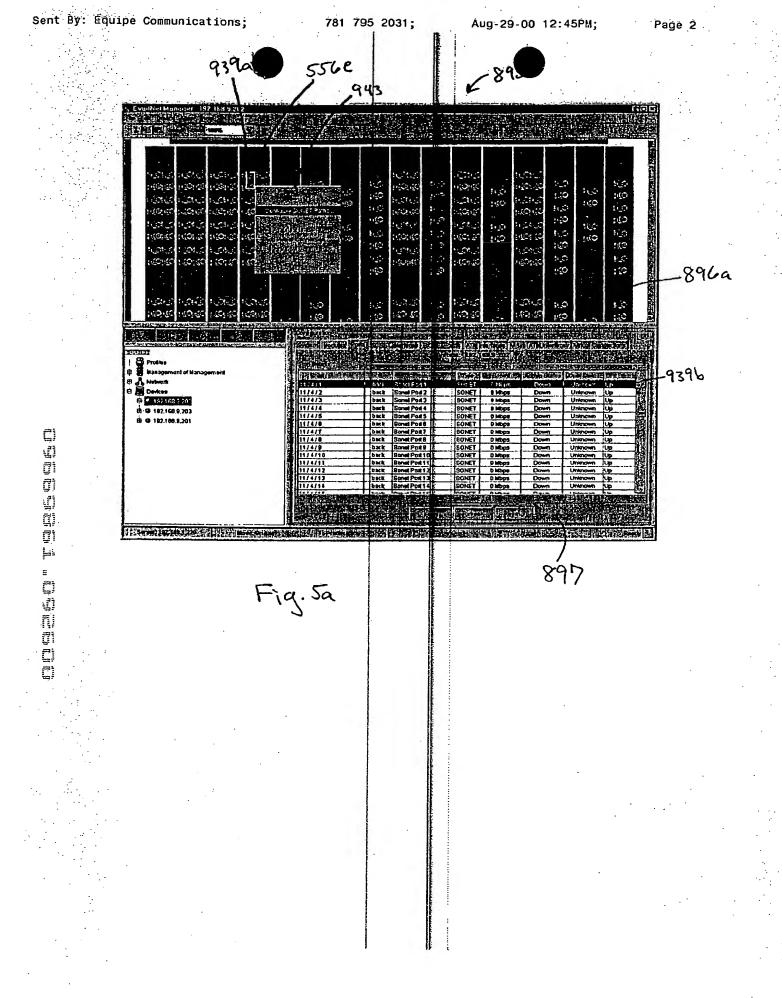
Fig.4u

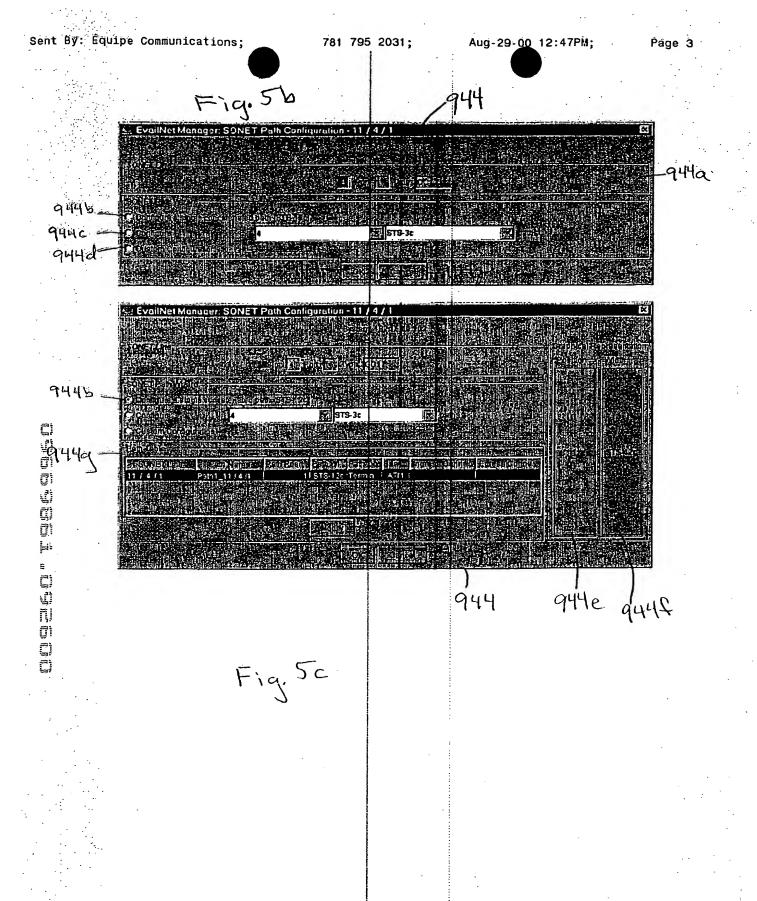


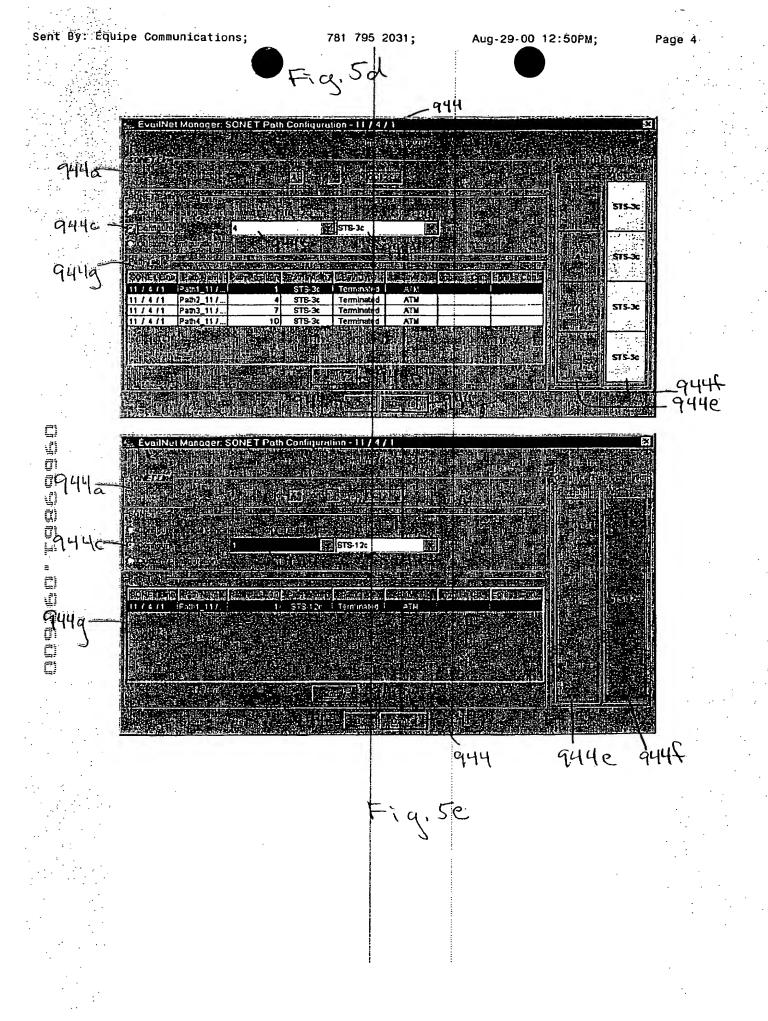


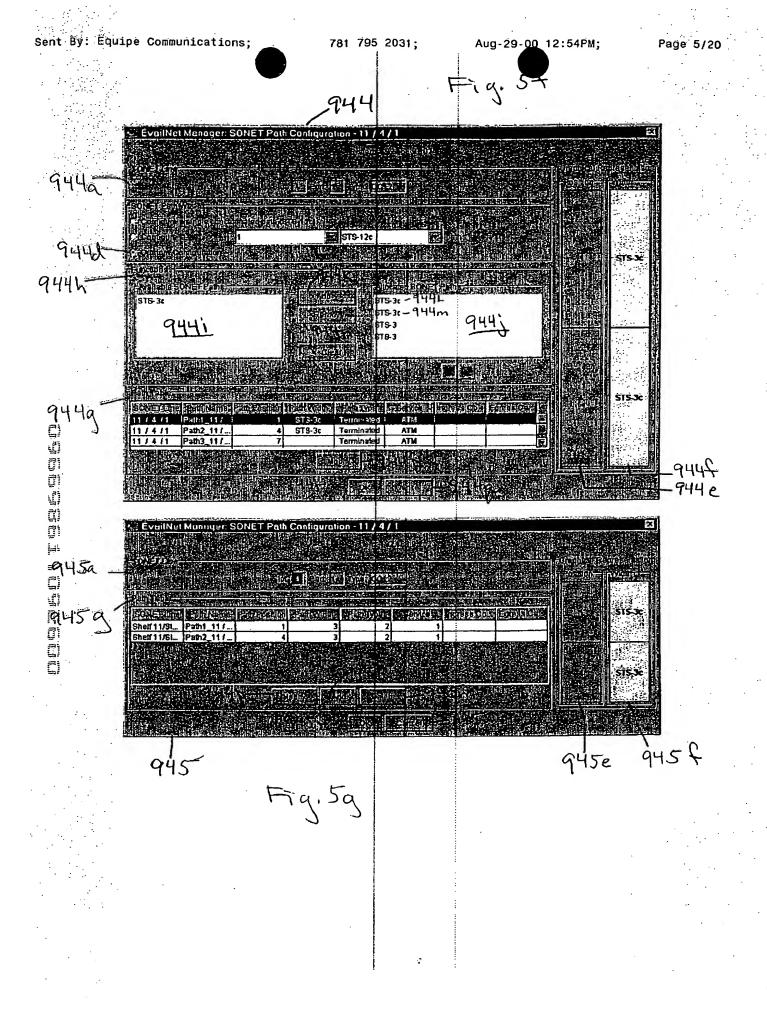


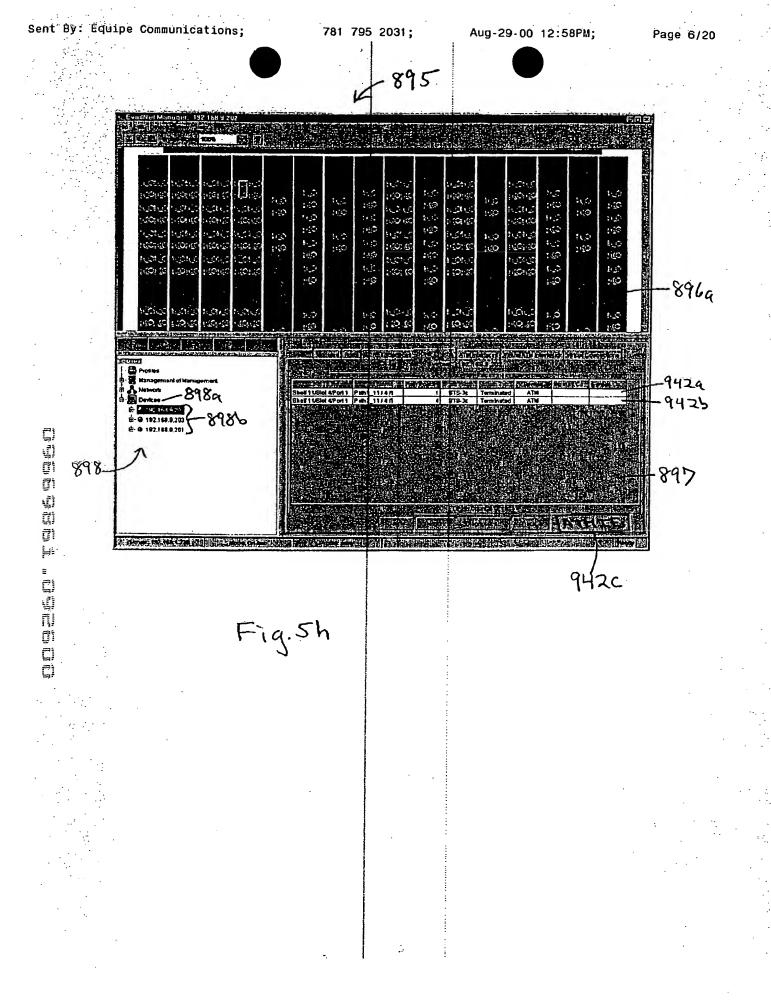


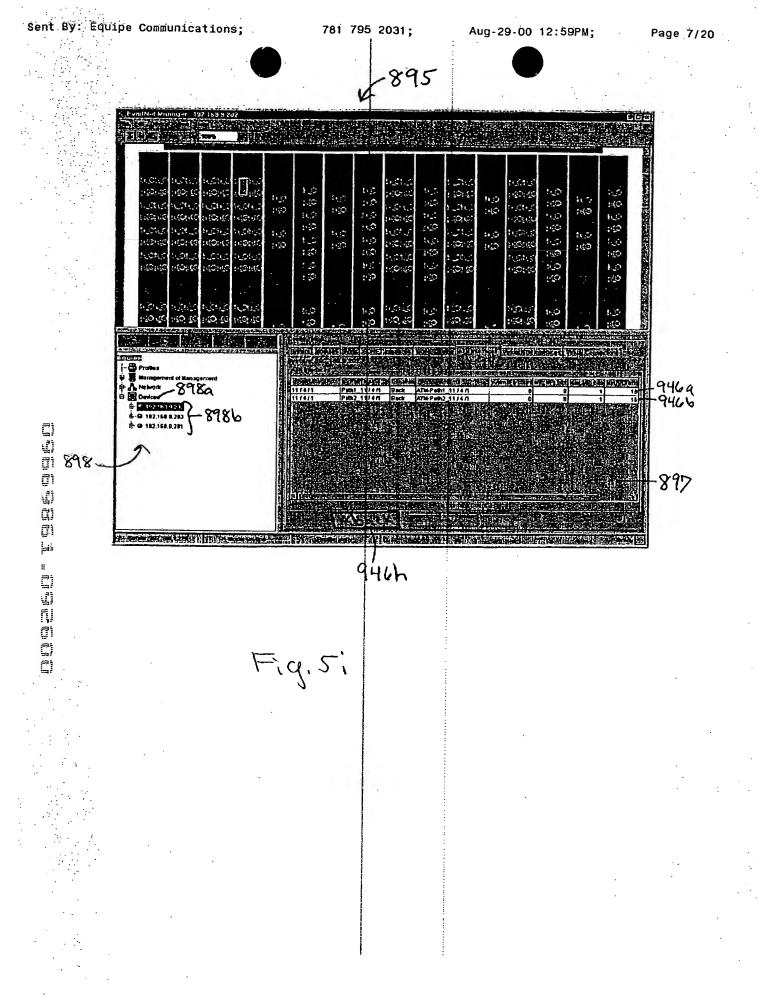


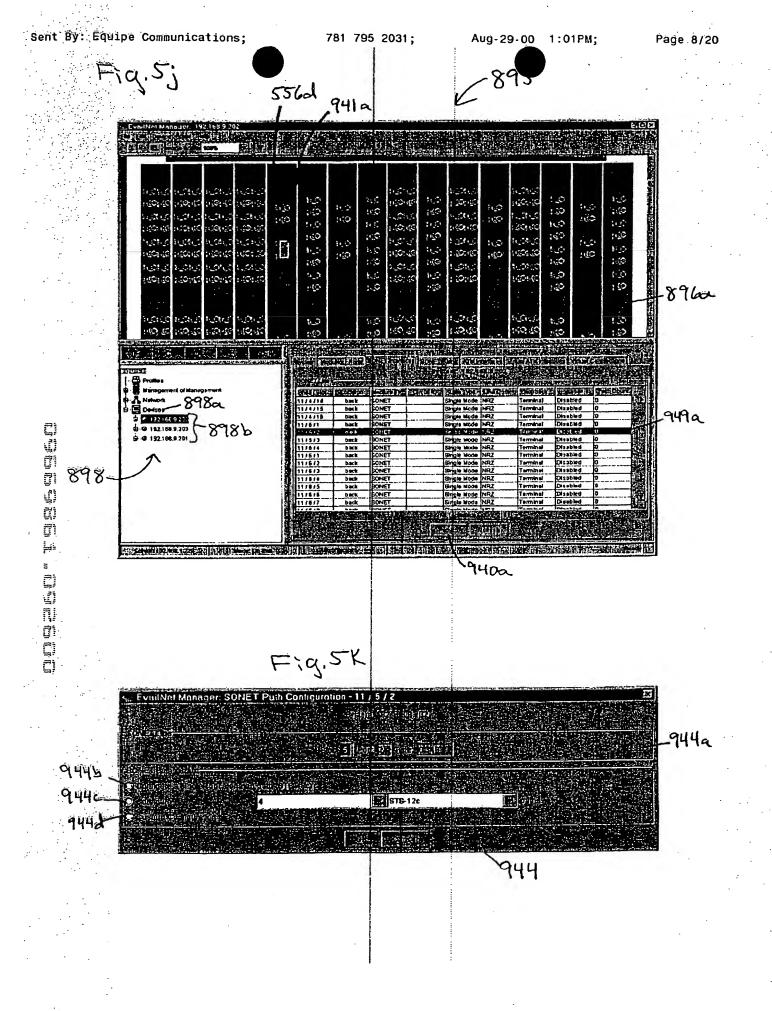


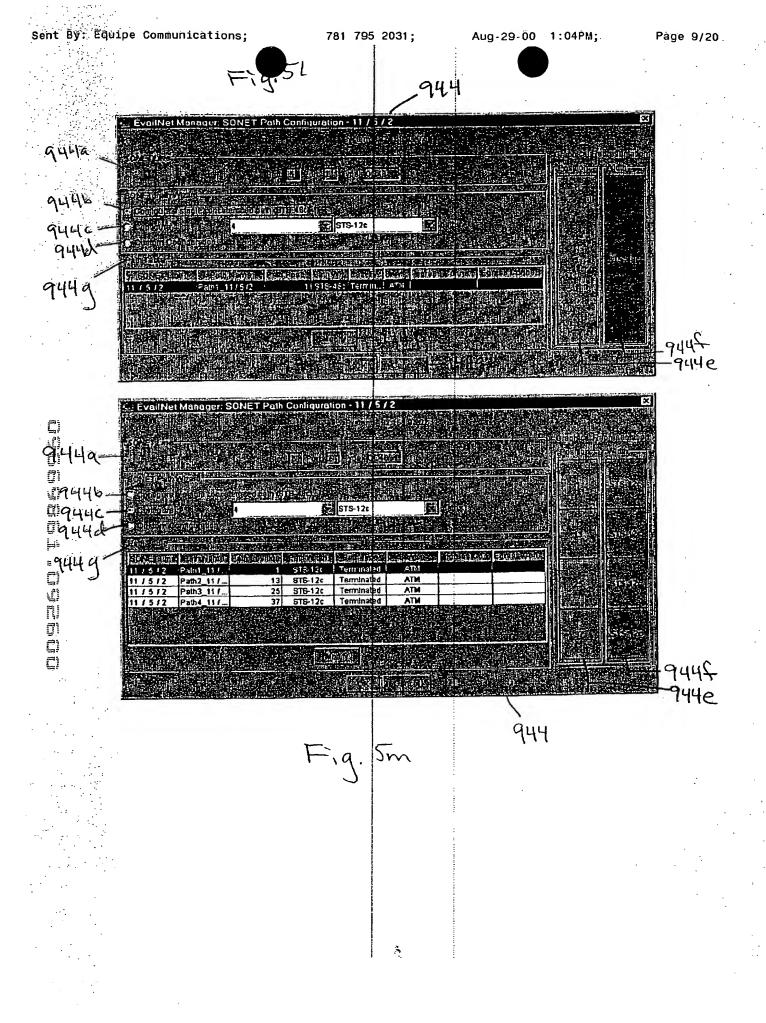


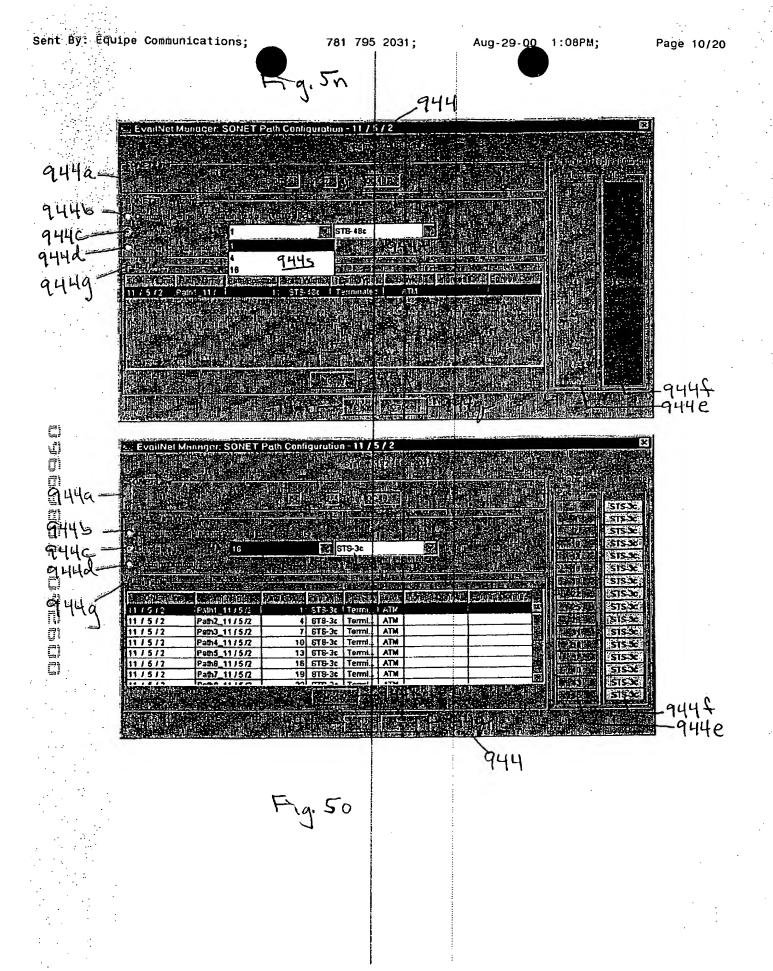


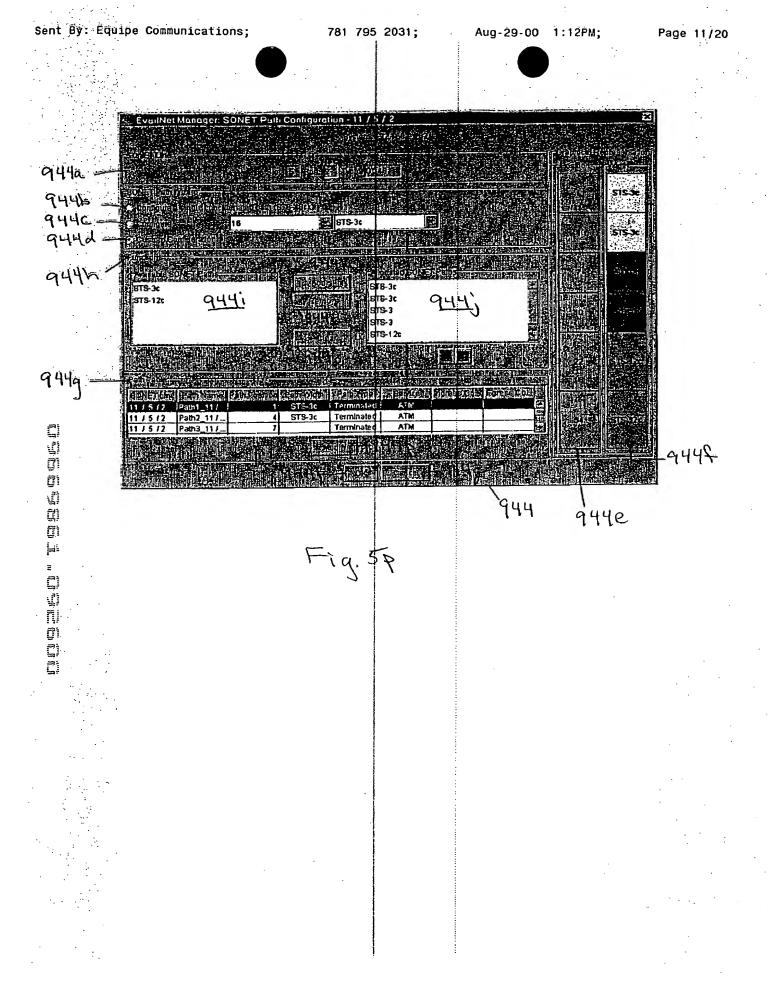


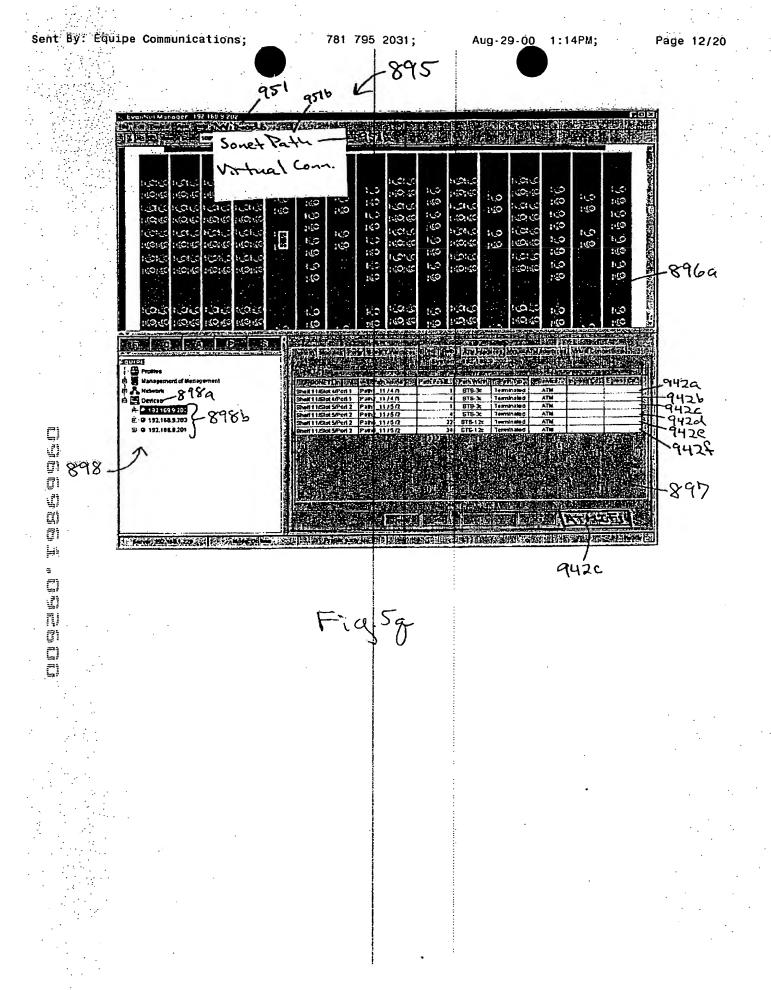


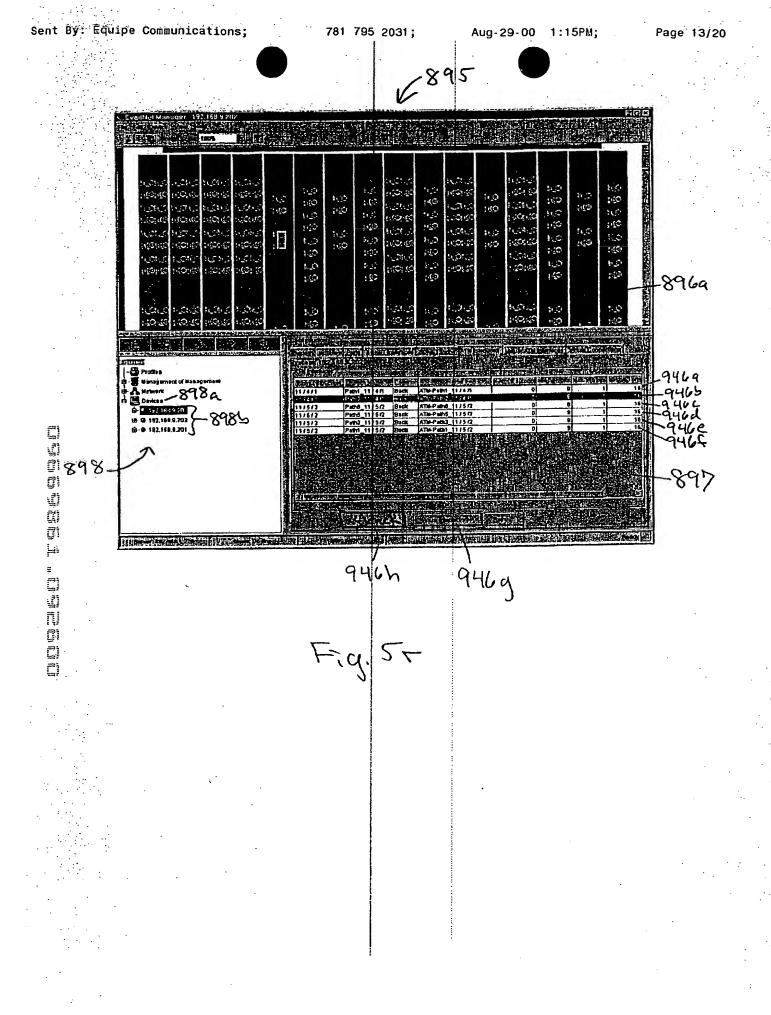












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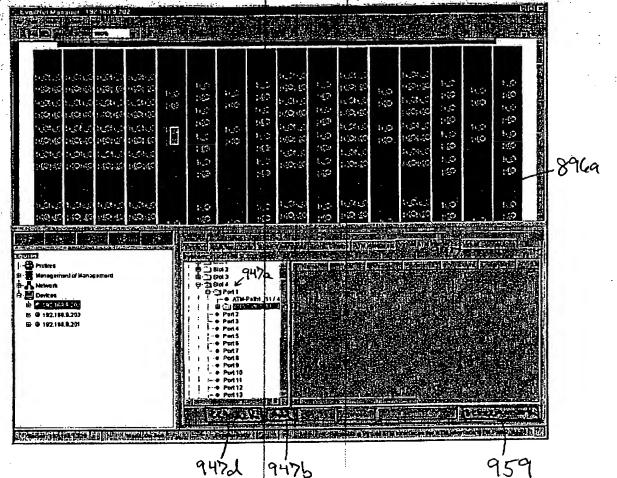
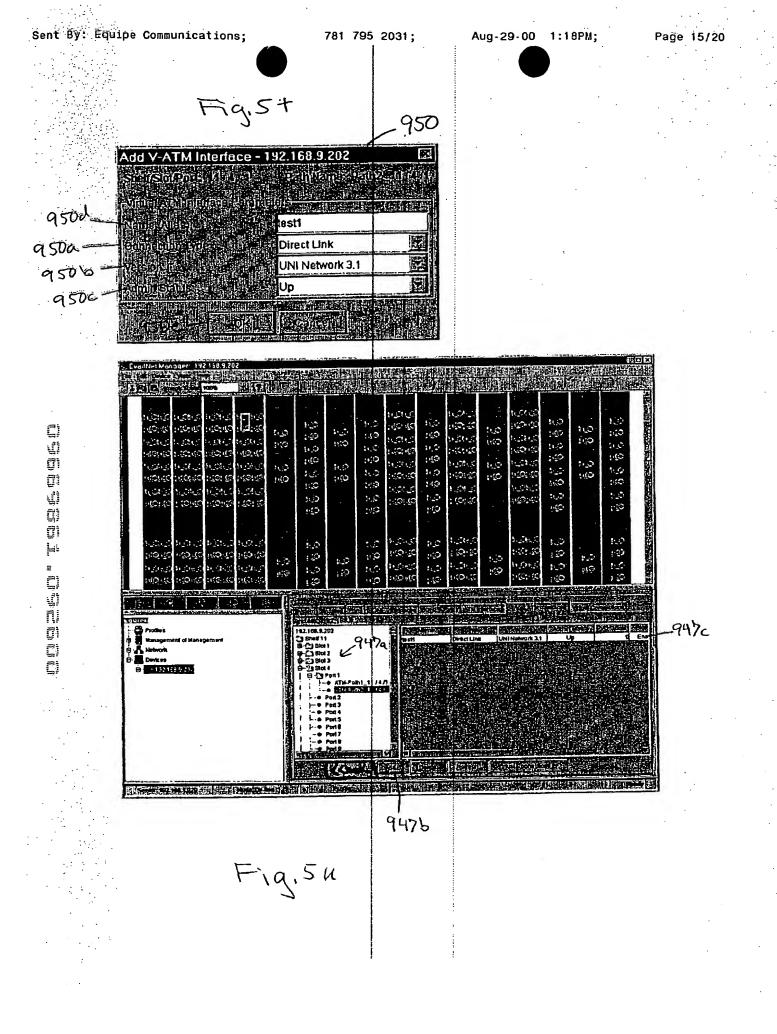
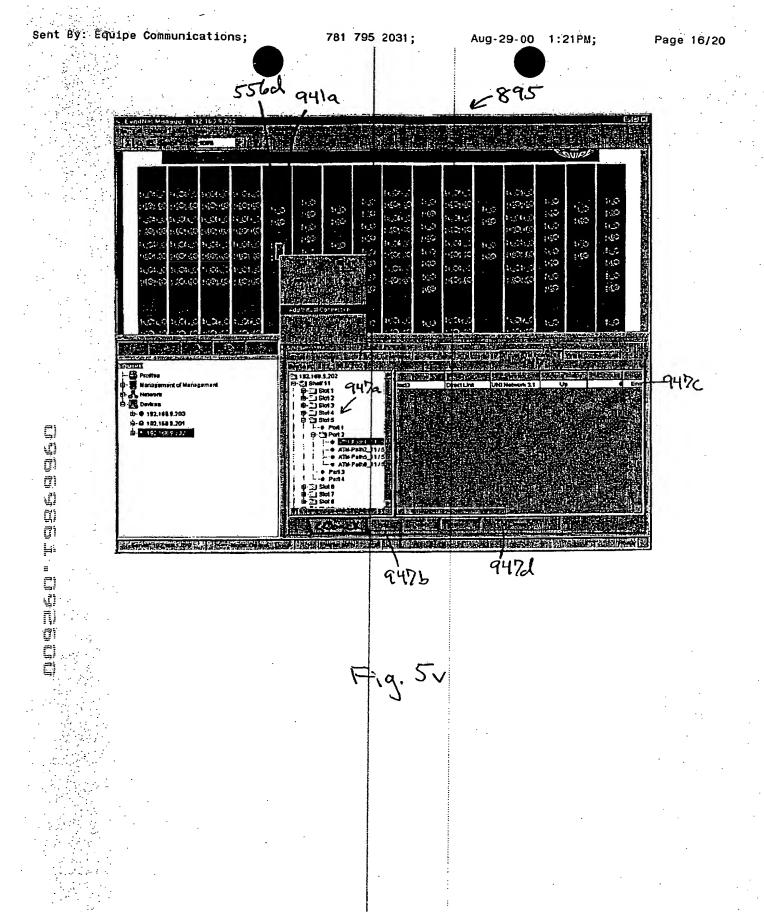


Fig. 5s





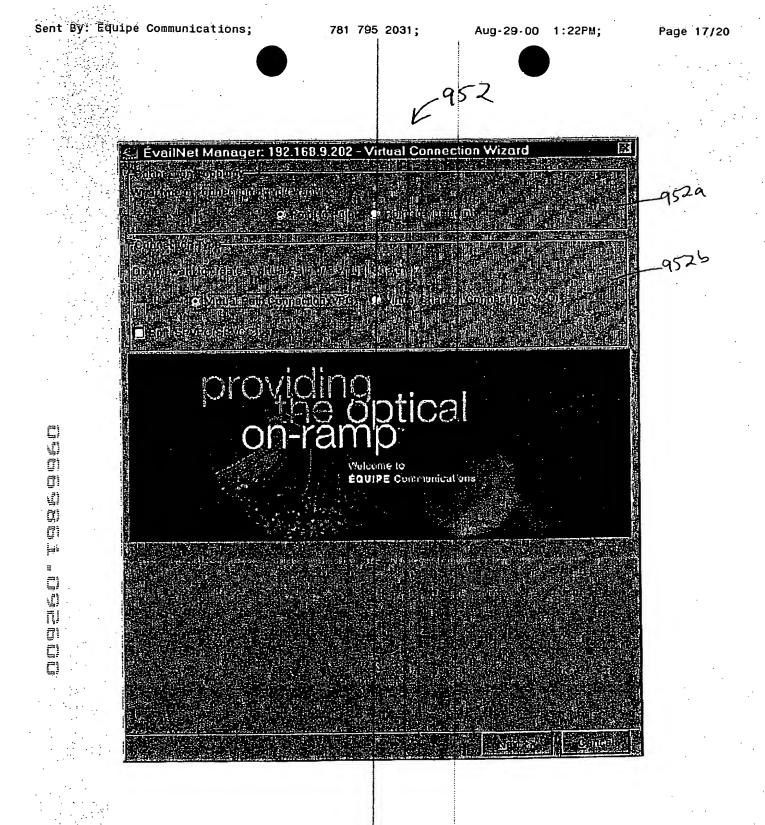
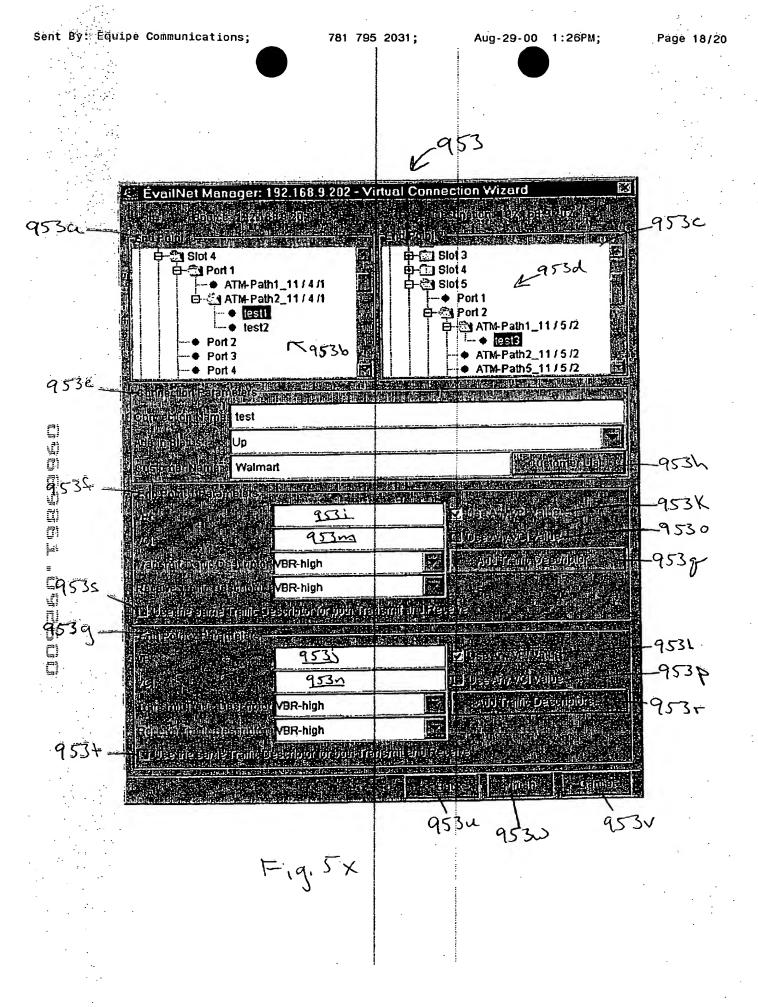
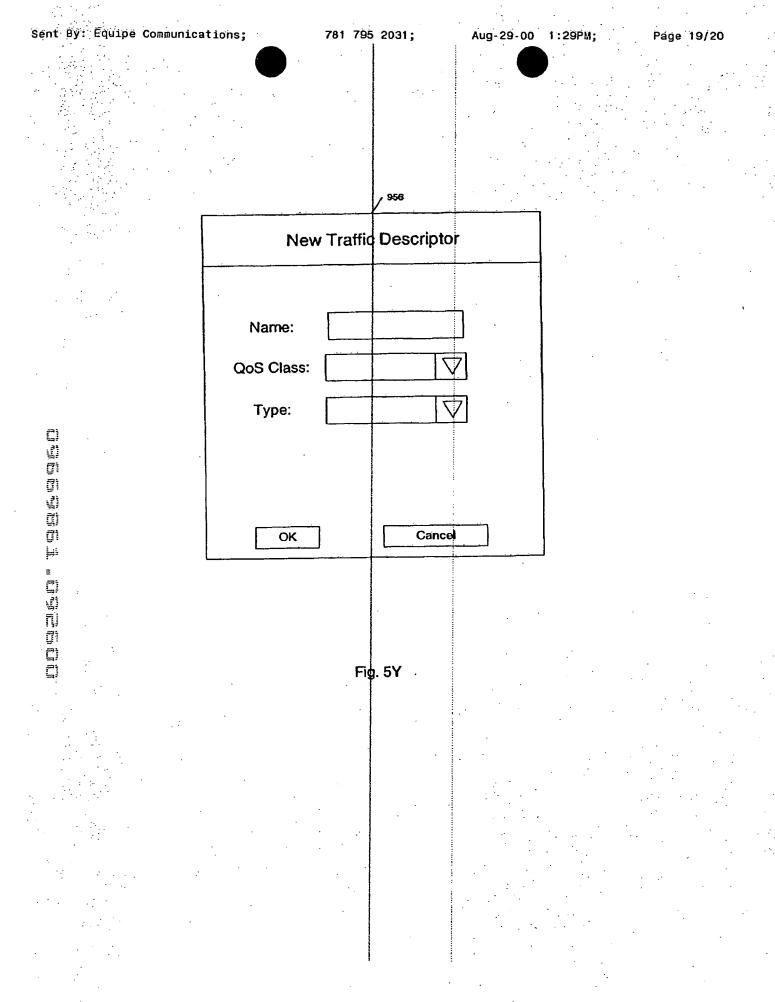
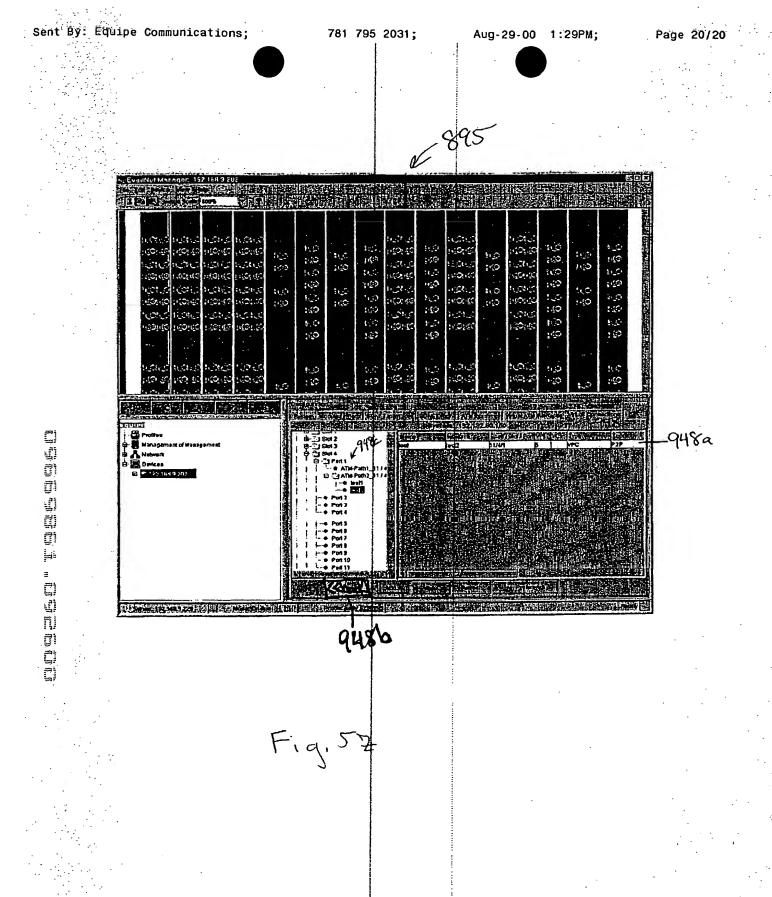


Fig. 5w







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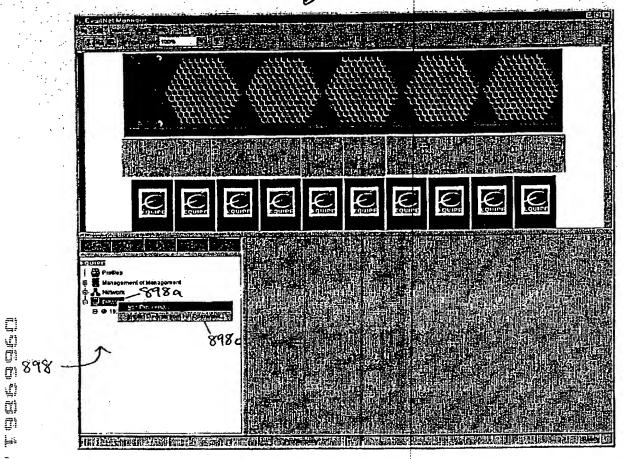


Fig. 6a



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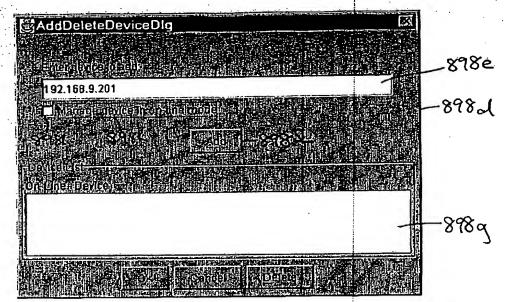
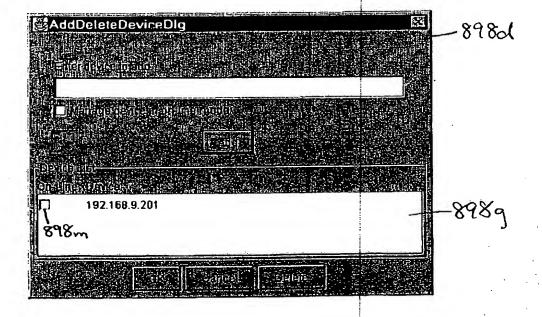


Fig.6c





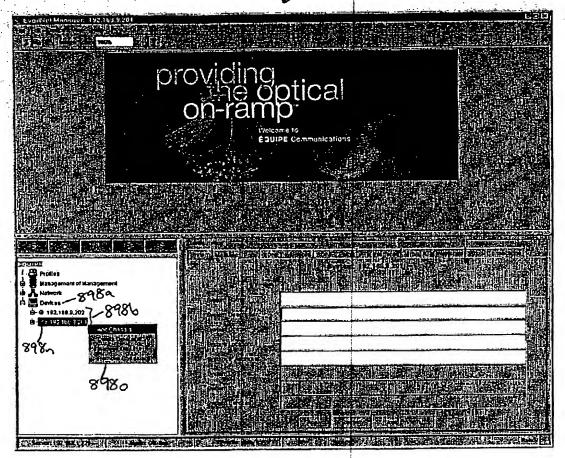


Fig.6d



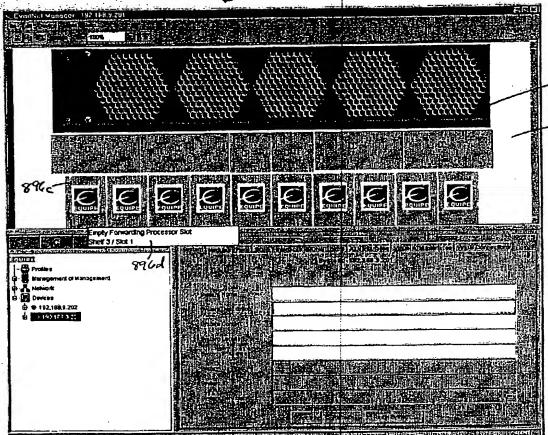


Fig. be

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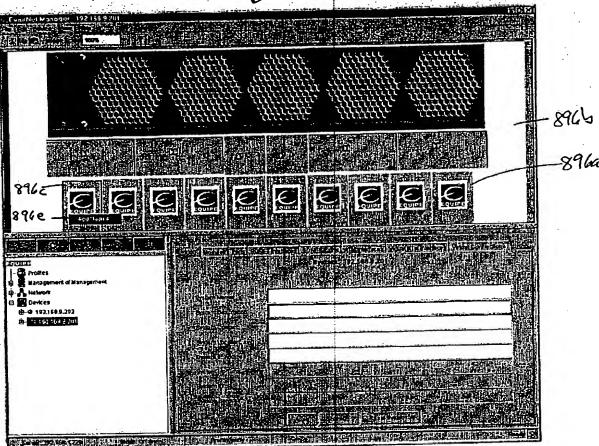


Fig.6f

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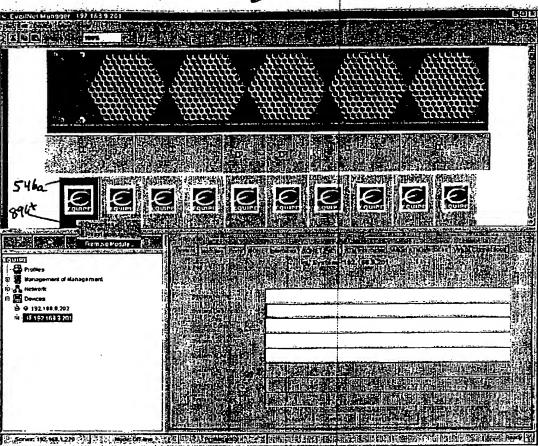
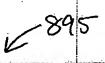


Fig. 69

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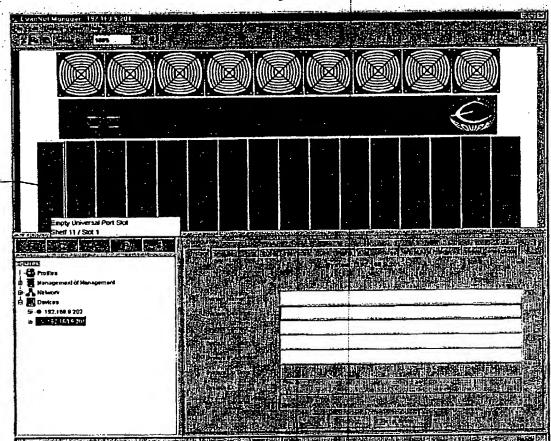
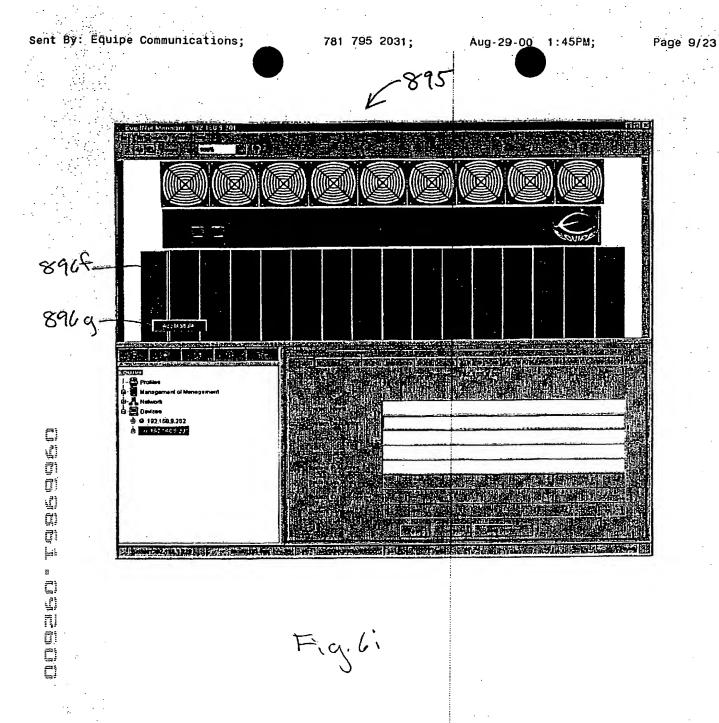
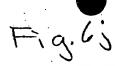
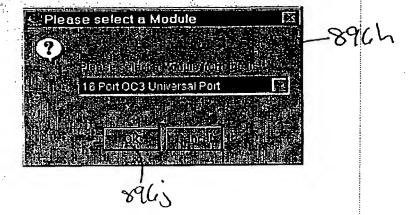


Fig.6h



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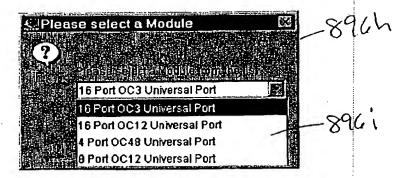


Fig. CK

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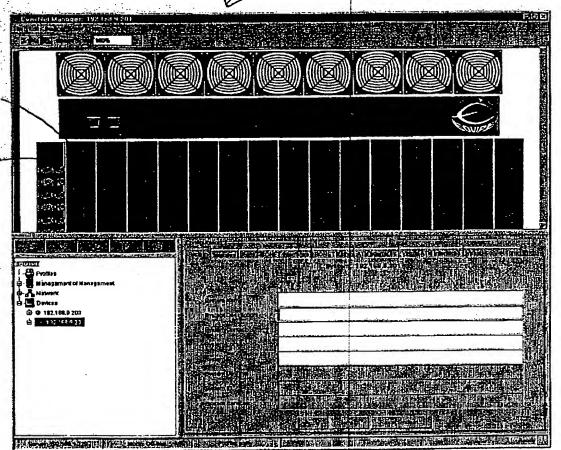


Fig. 6L

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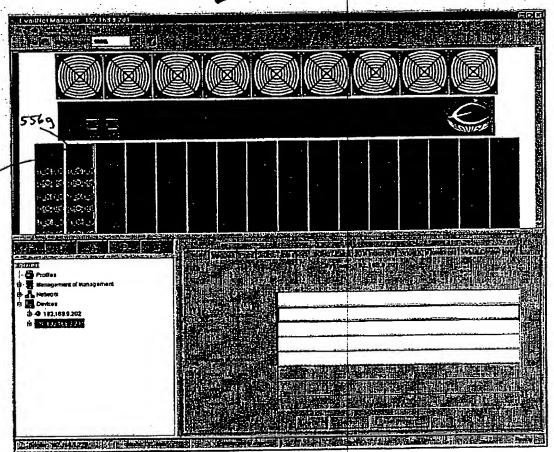


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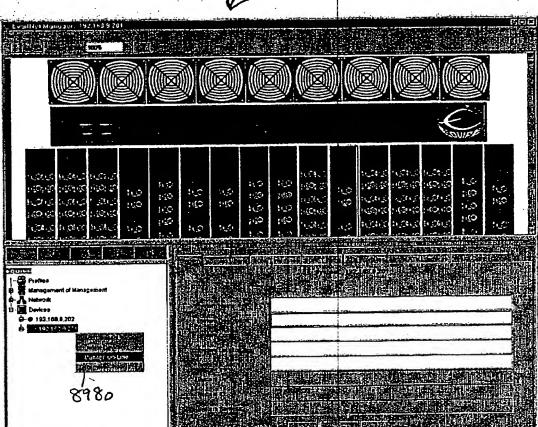


Fig. 6n

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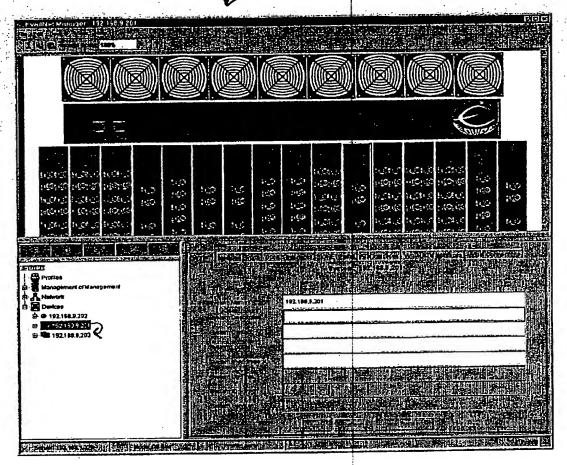


Fig. 60

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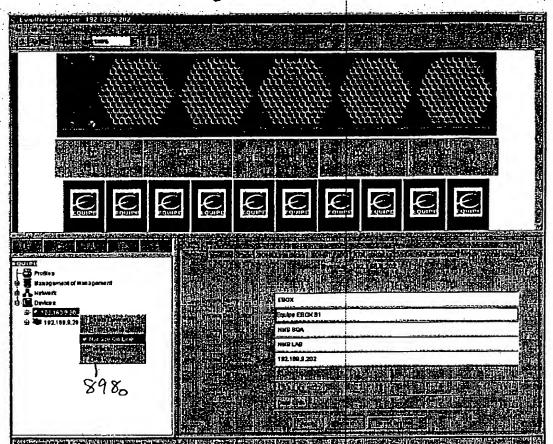
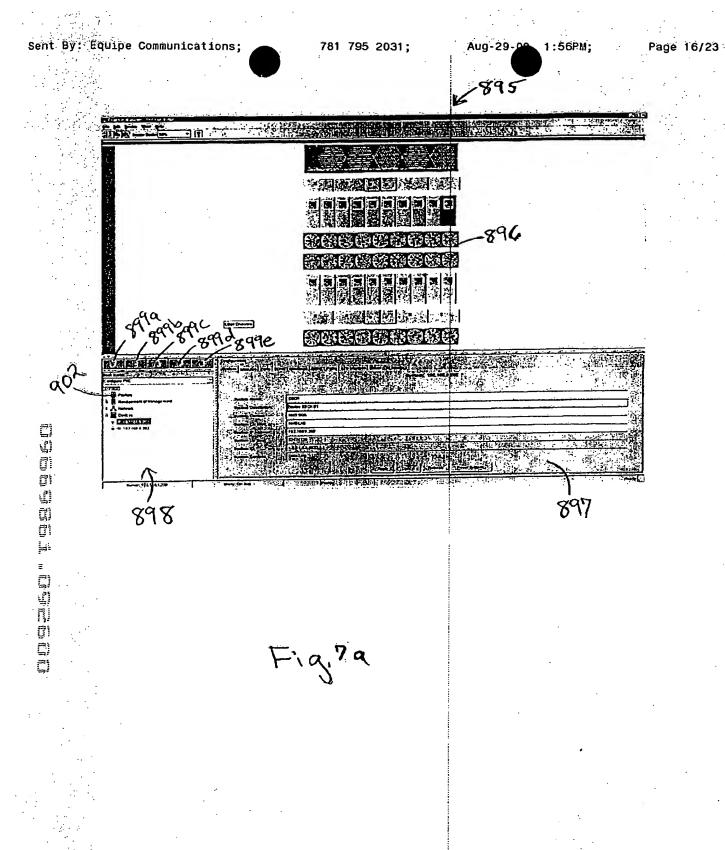


Fig. 6P





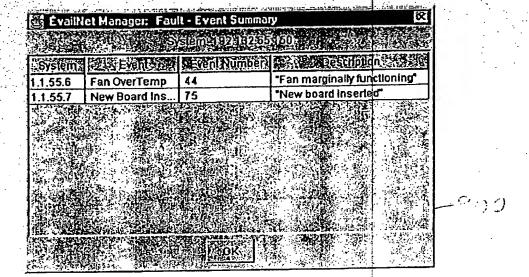


Fig. 76

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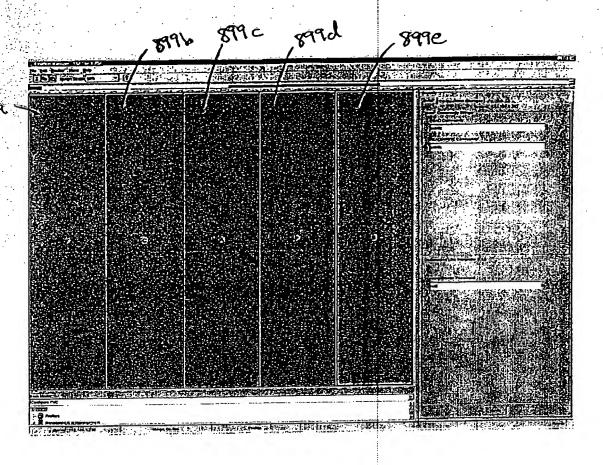


Fig.7c

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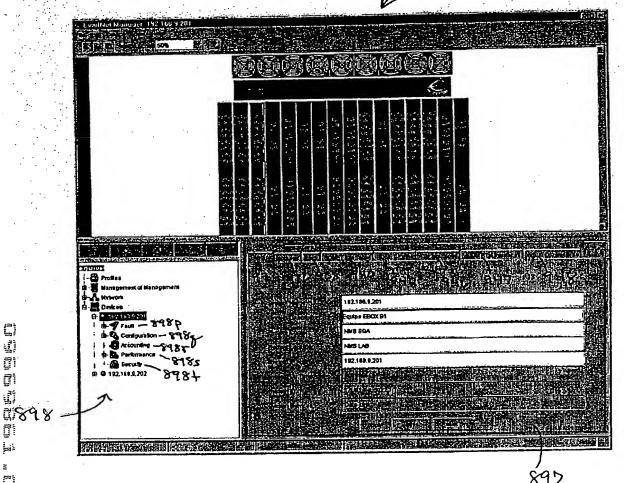
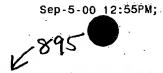


Fig.7d



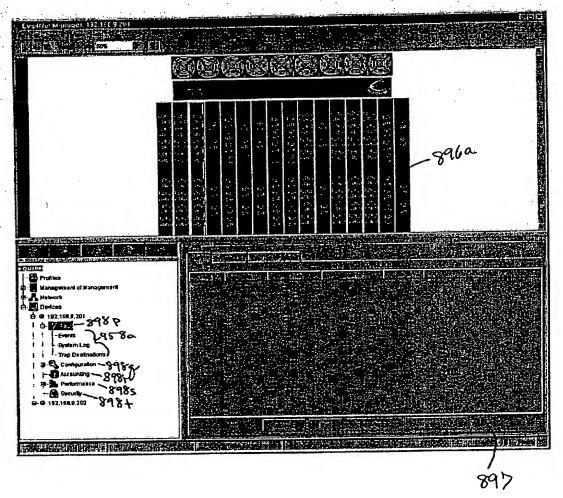
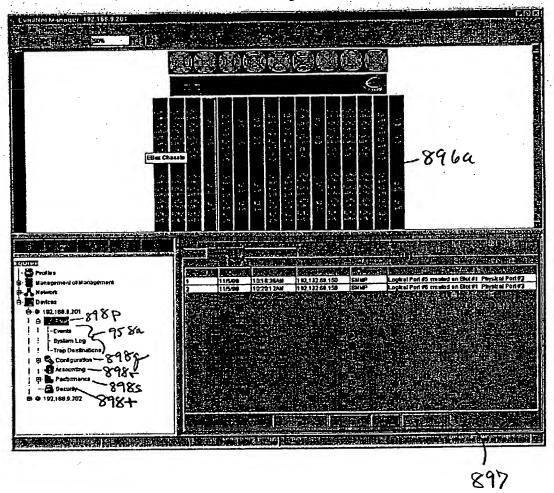


Fig. 7e

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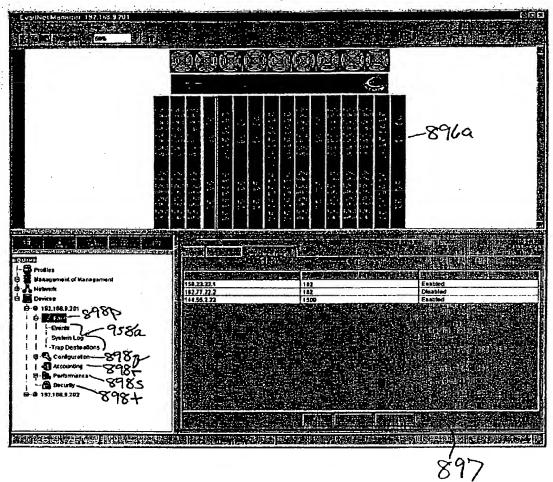
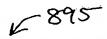


Fig. 79



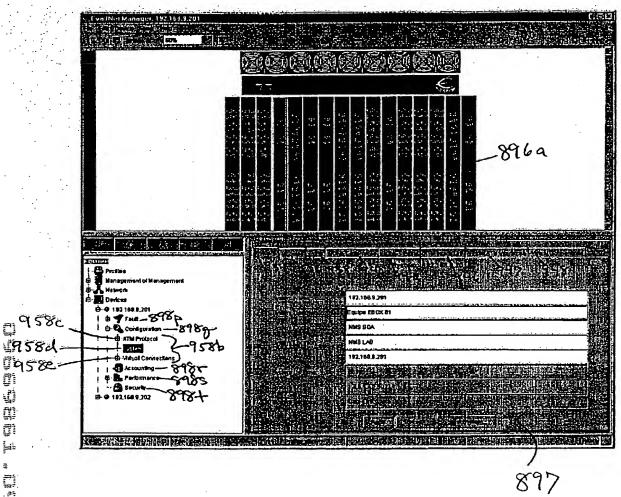
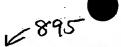


Fig. M

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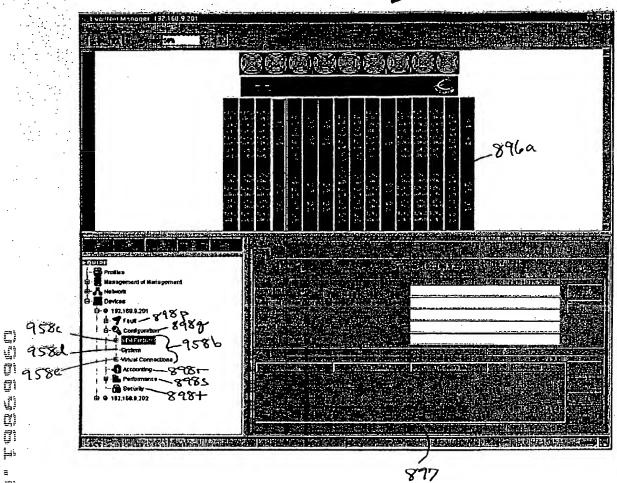


Fig. 7:

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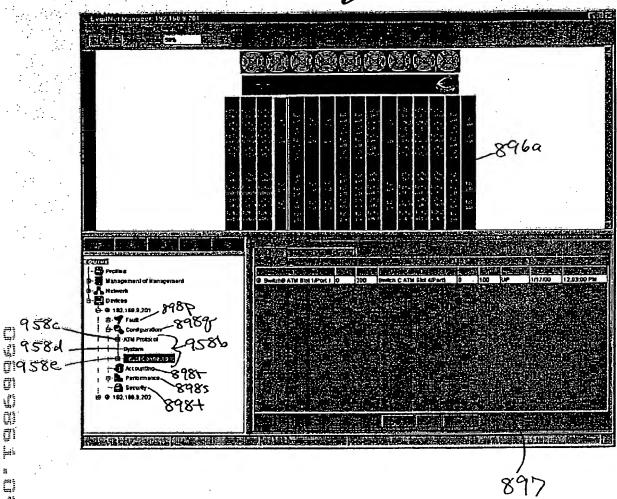


Fig. 7;

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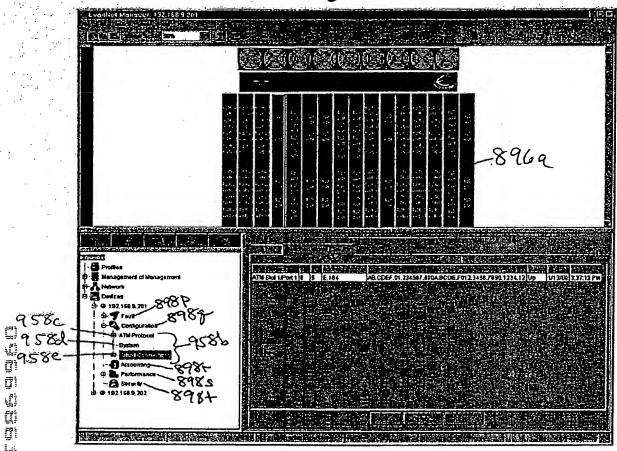


Fig. 7K

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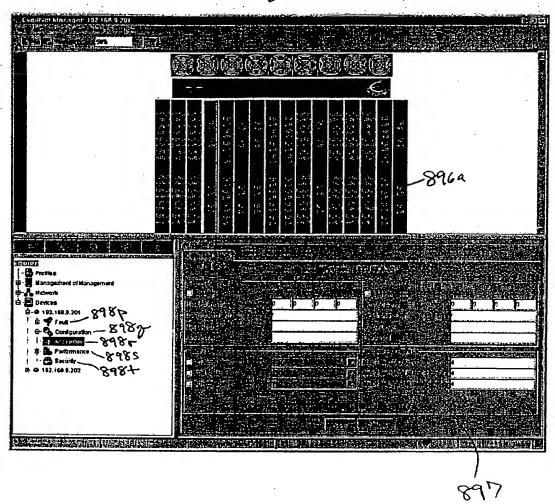


Fig.7L

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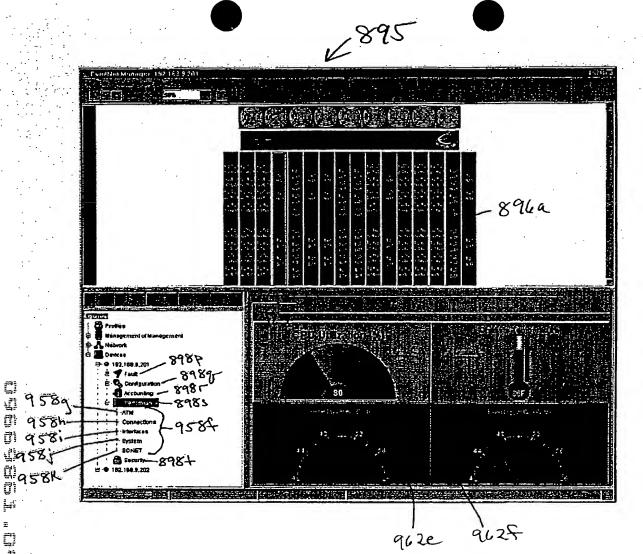


Fig.7m

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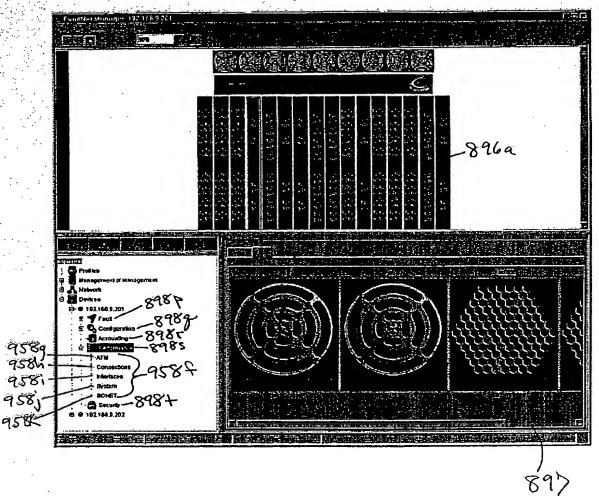


Fig. m



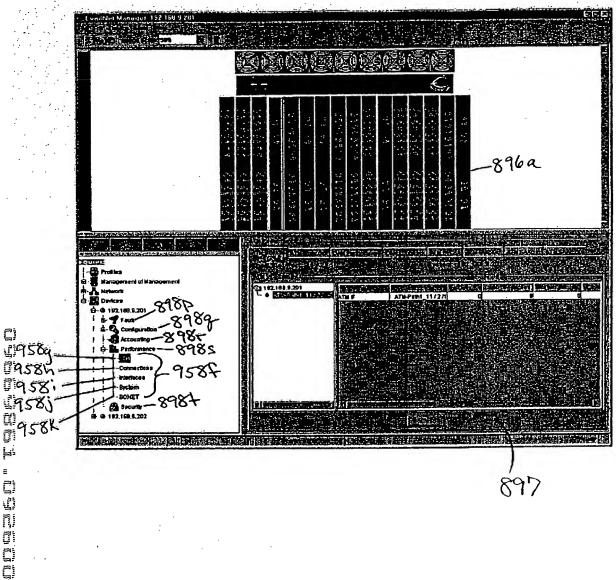
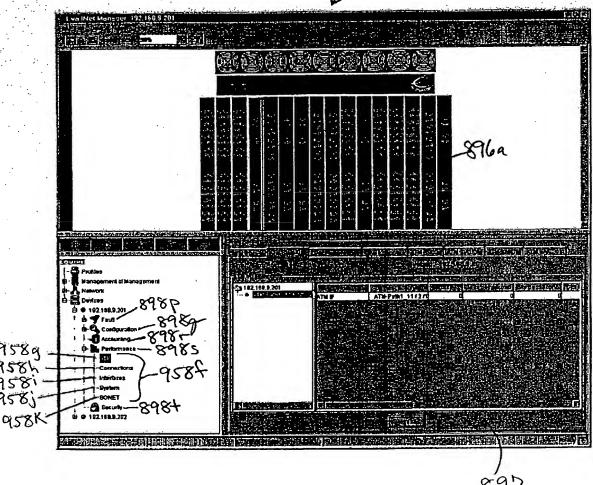


Fig. 70

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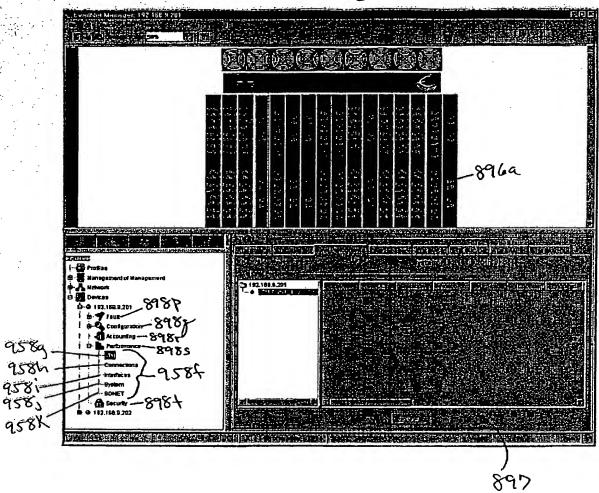


Fig. 7g

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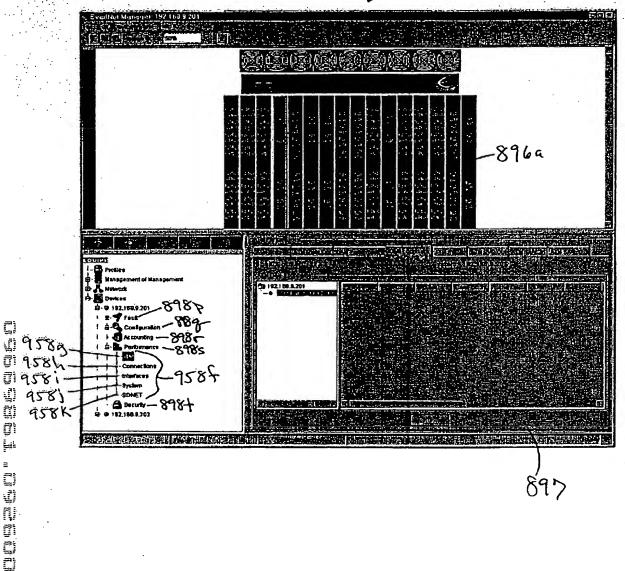


Fig. 7r

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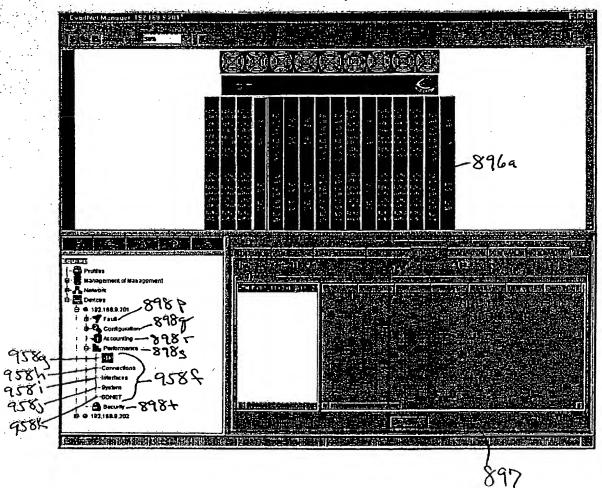
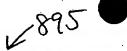


Fig. 7s

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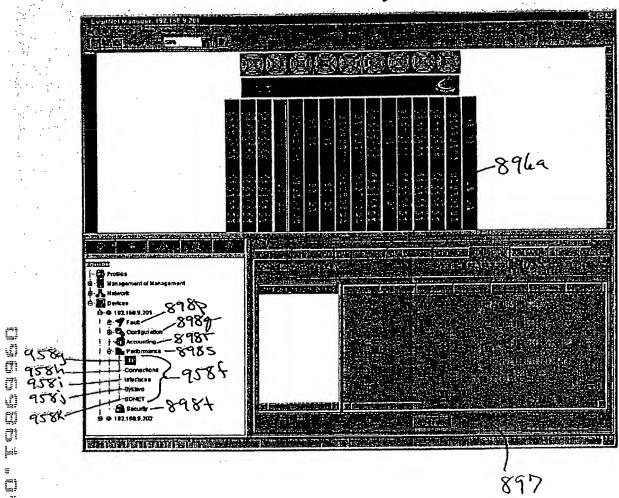
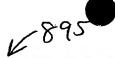


Fig. 7+

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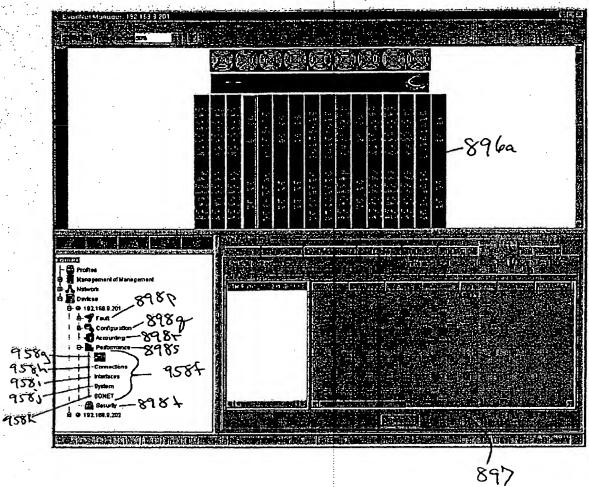
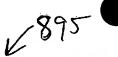
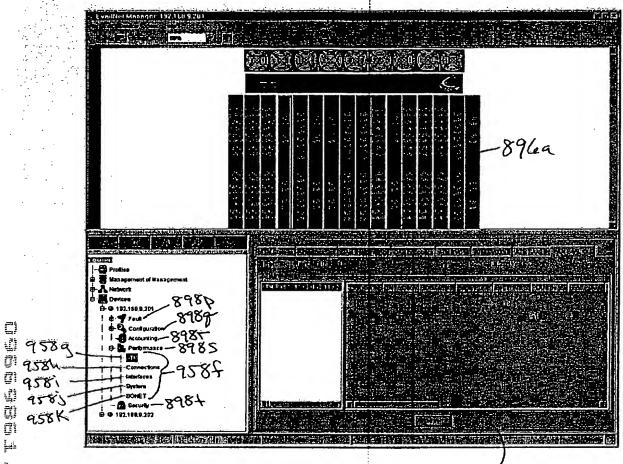
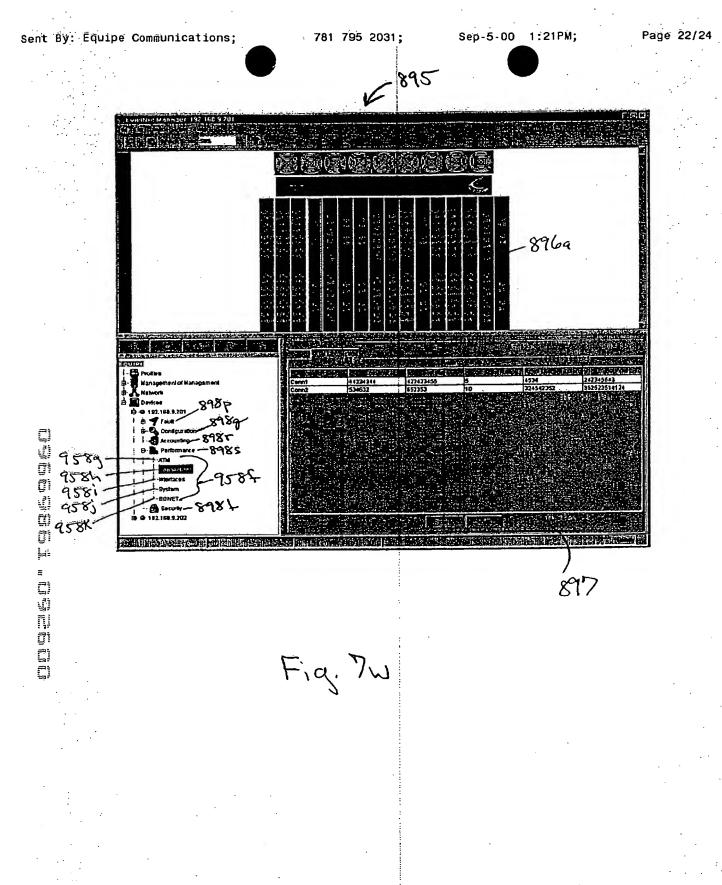
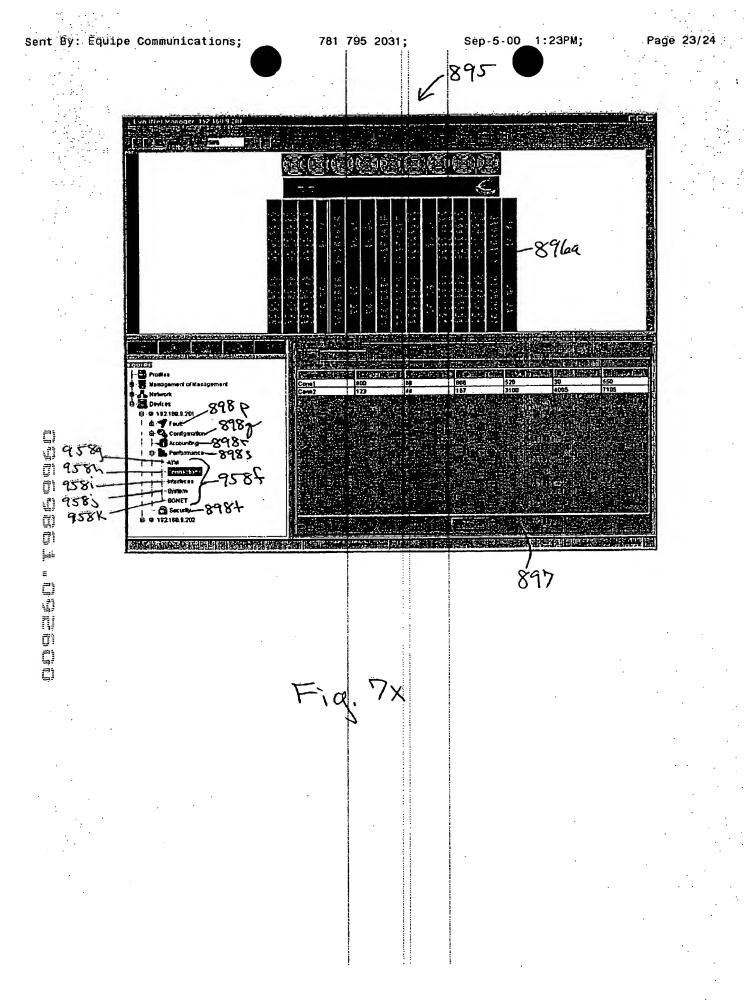


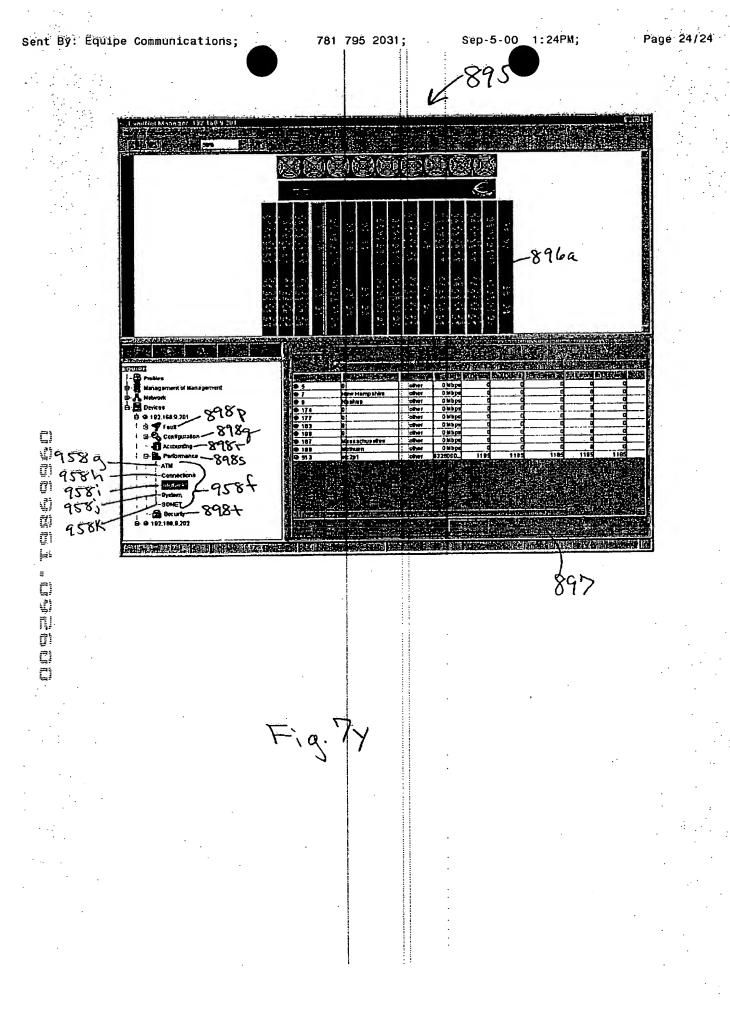
Fig. 7u



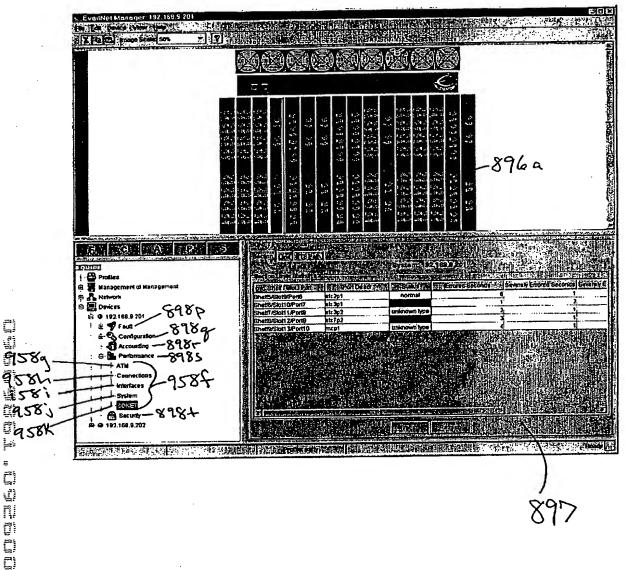






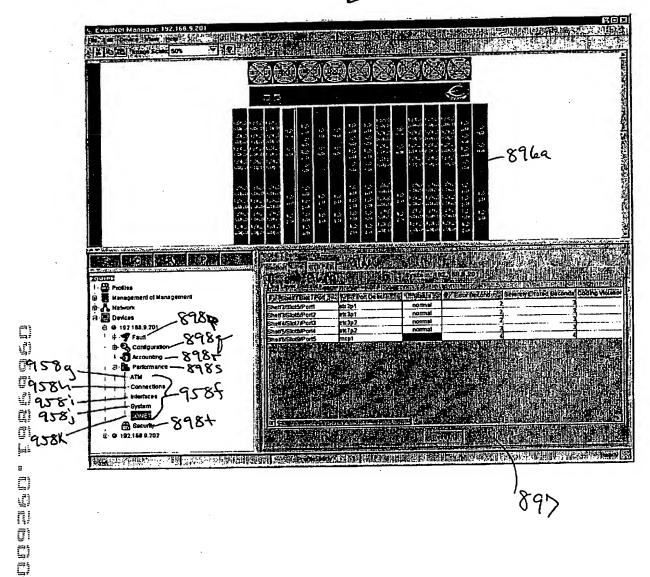


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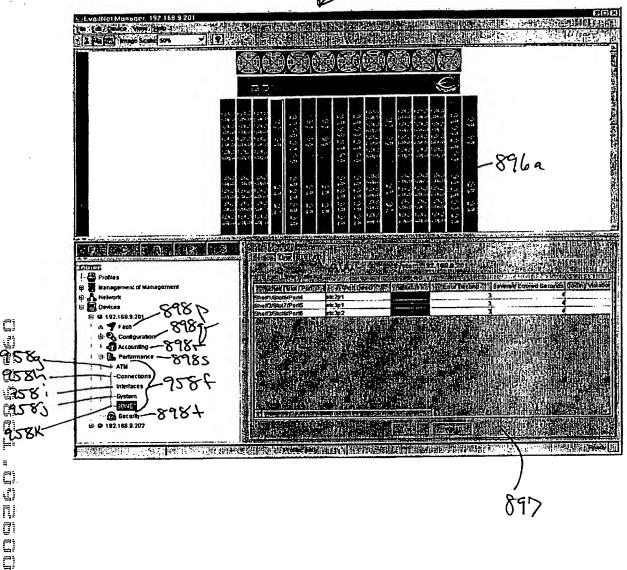
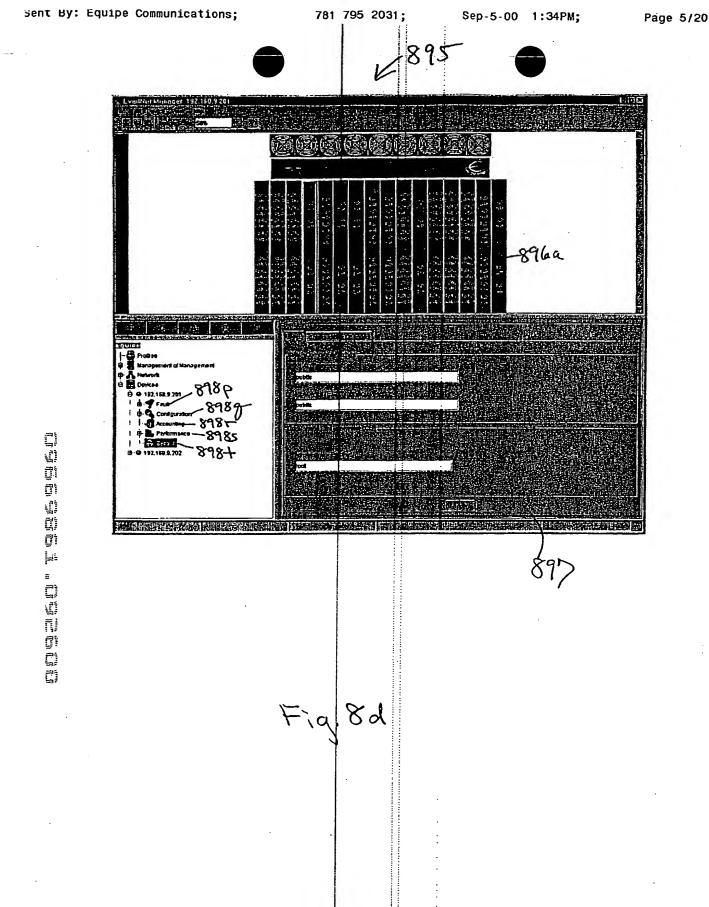
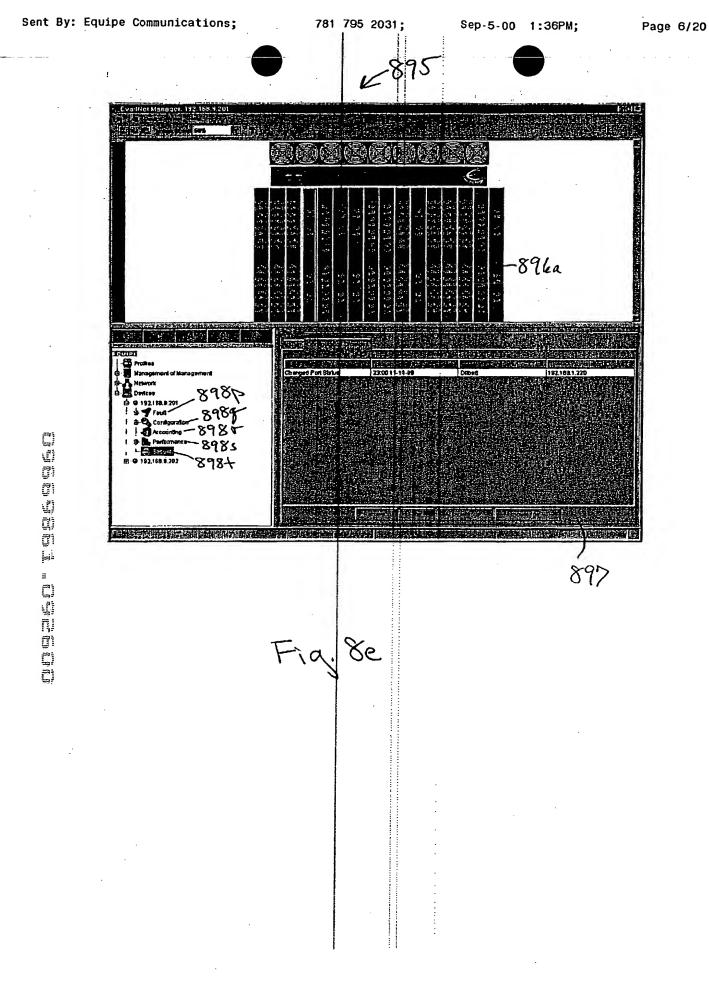
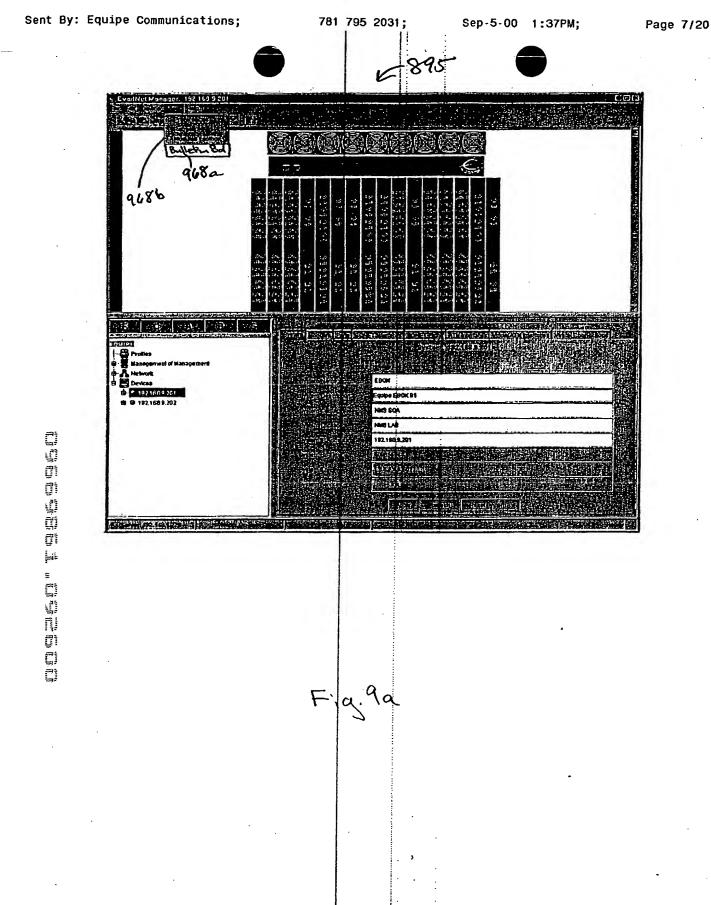
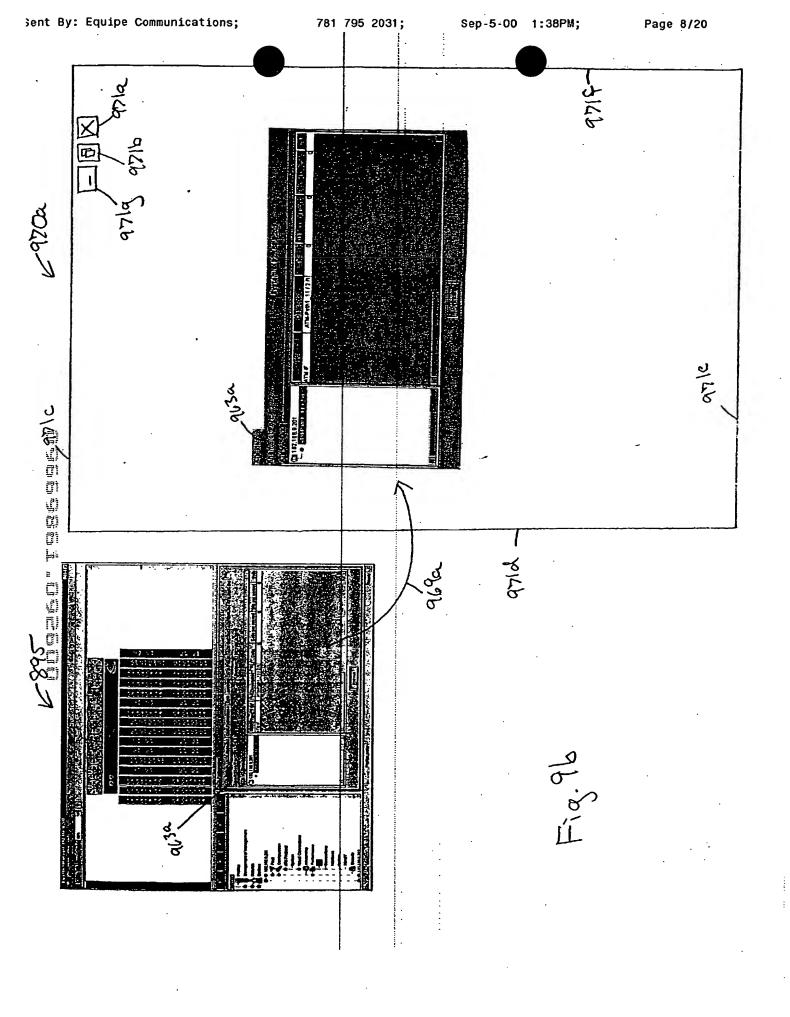


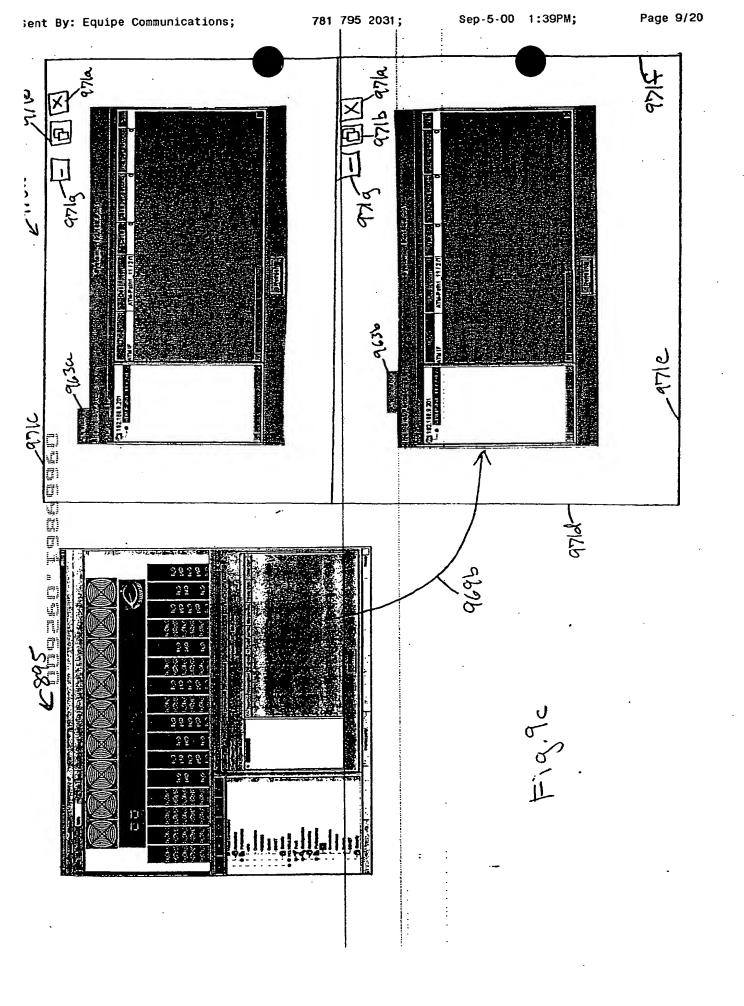
Fig. 8c

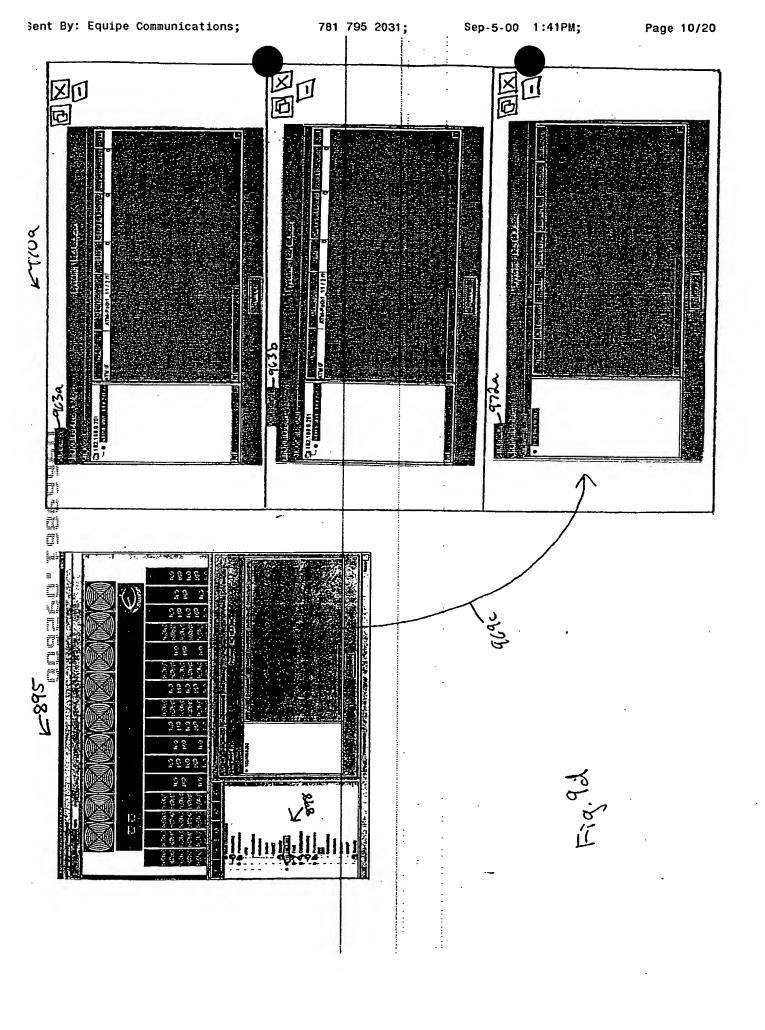


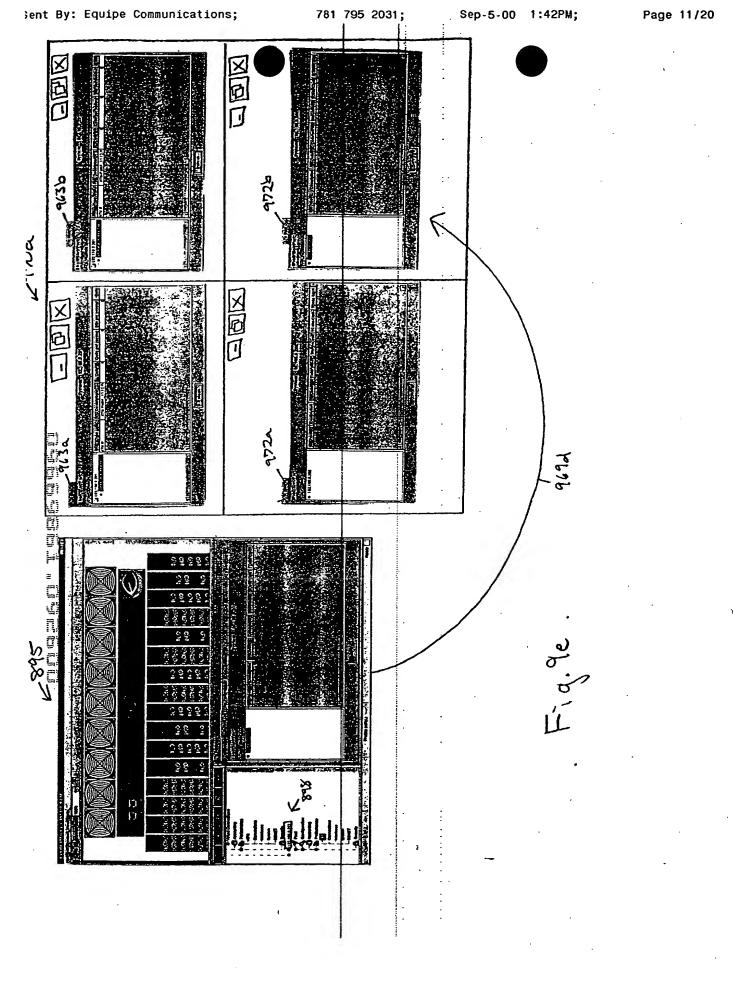


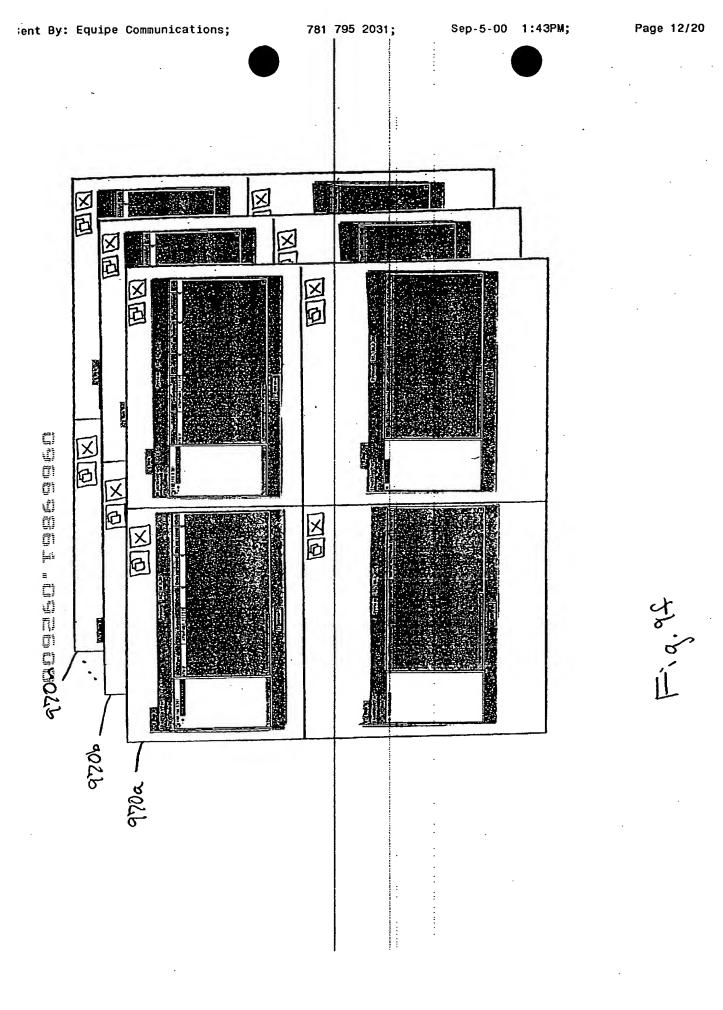


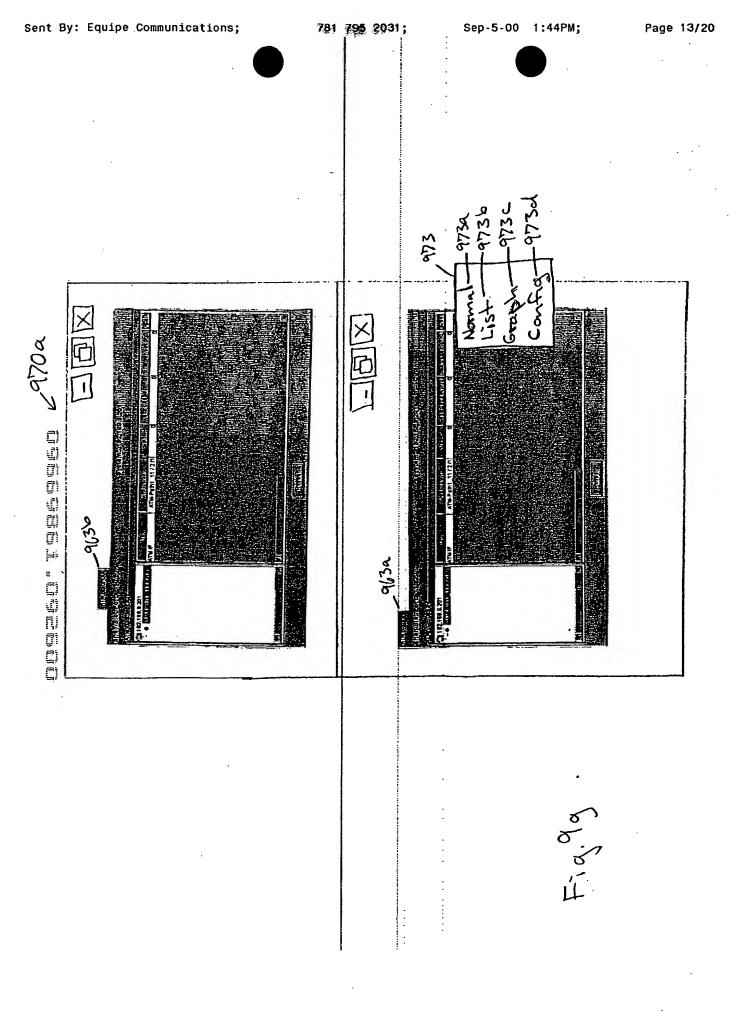


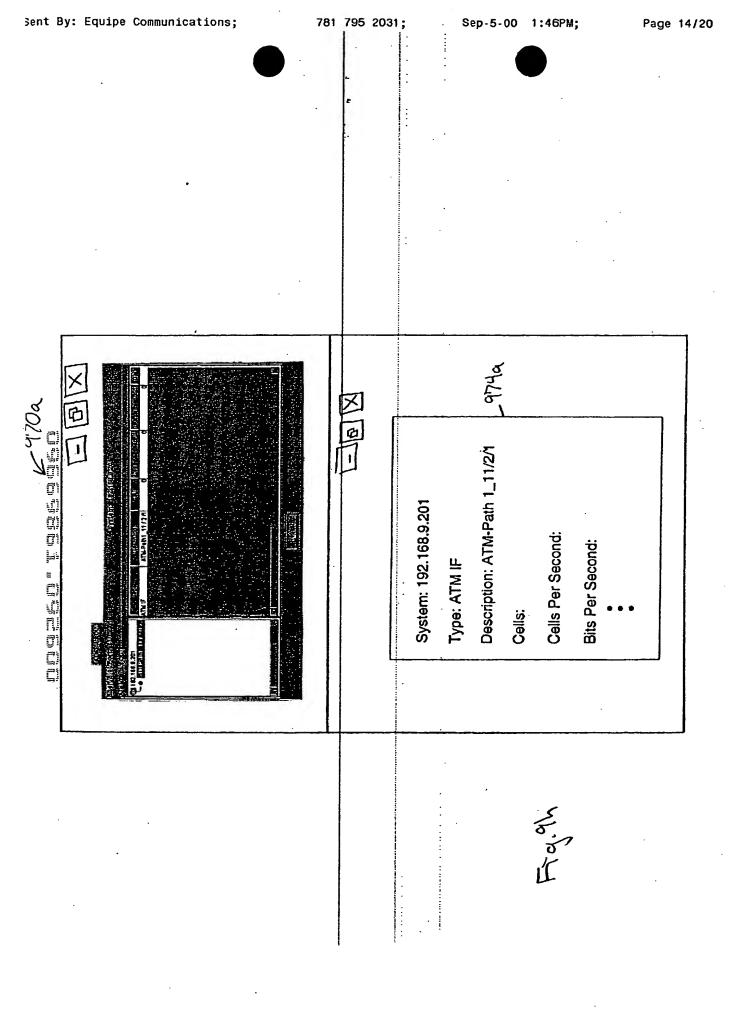


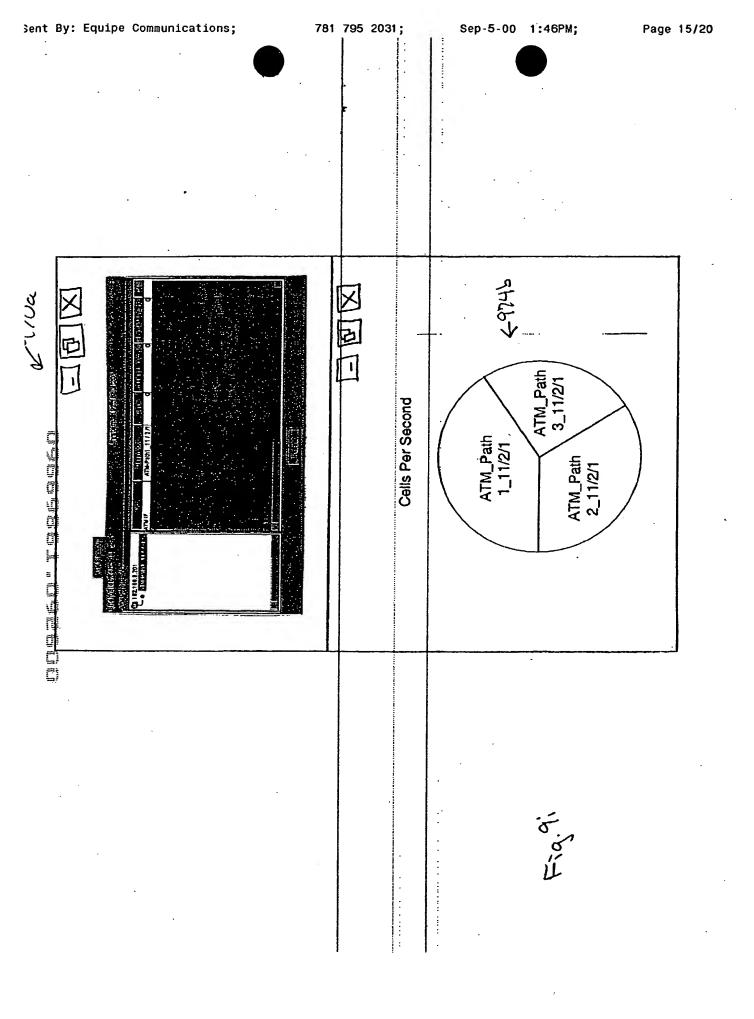


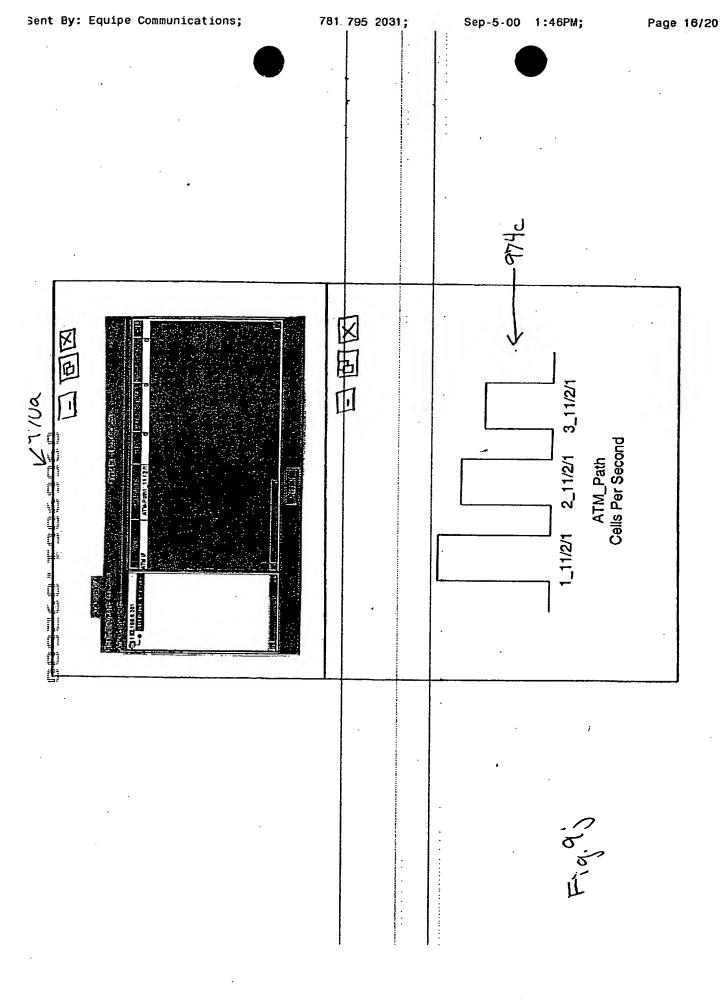


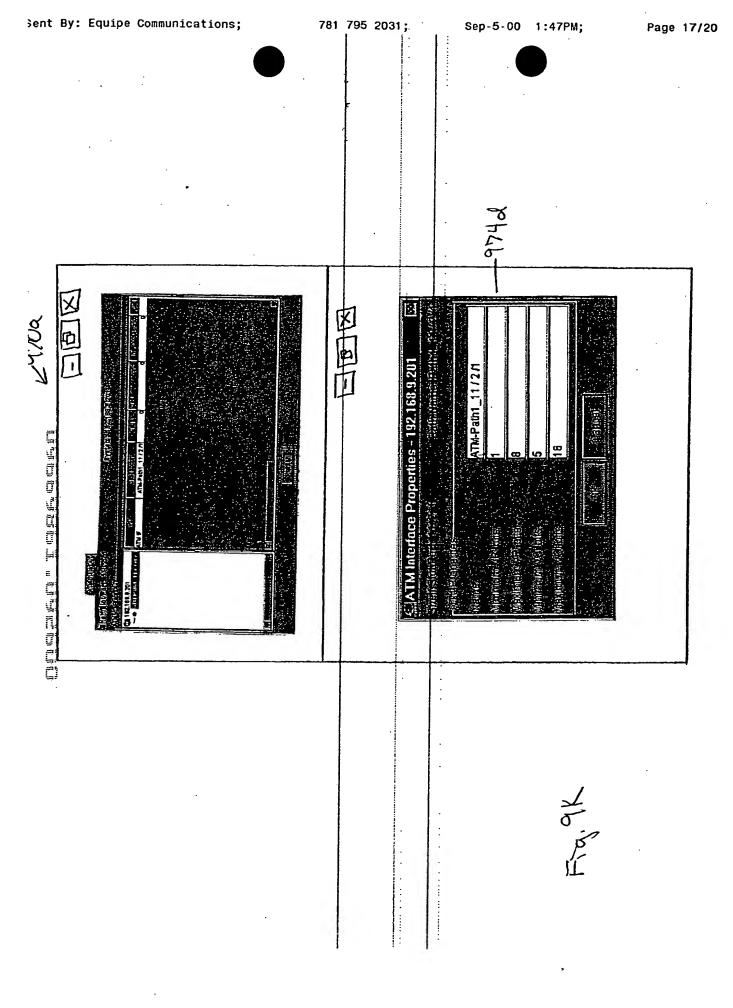


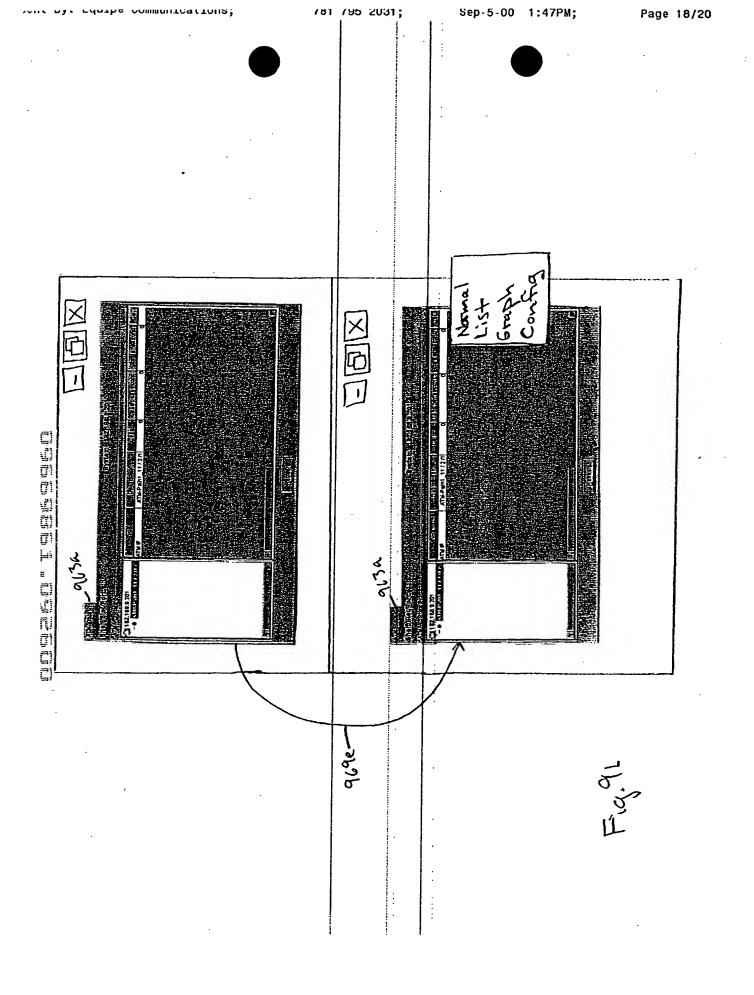


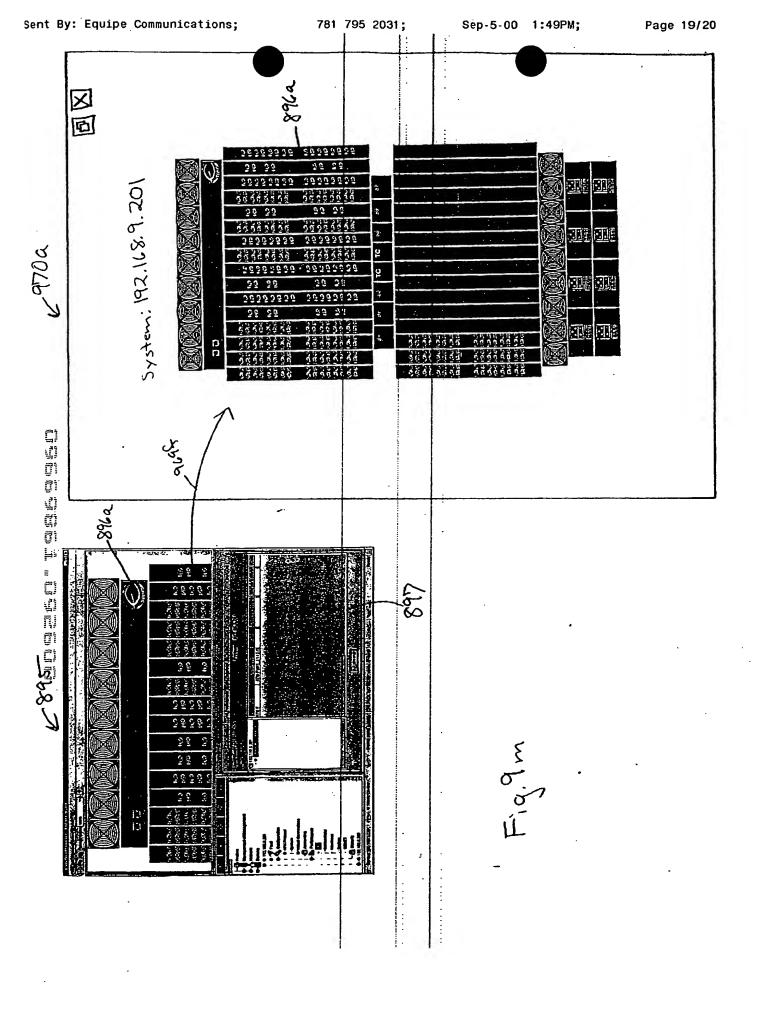


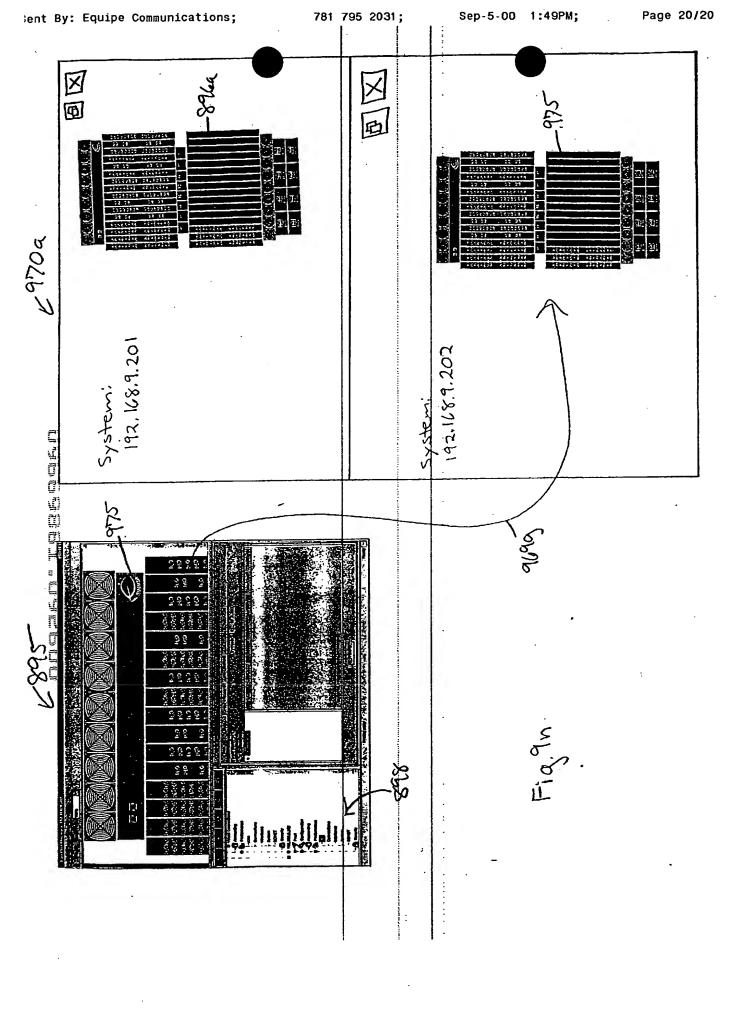


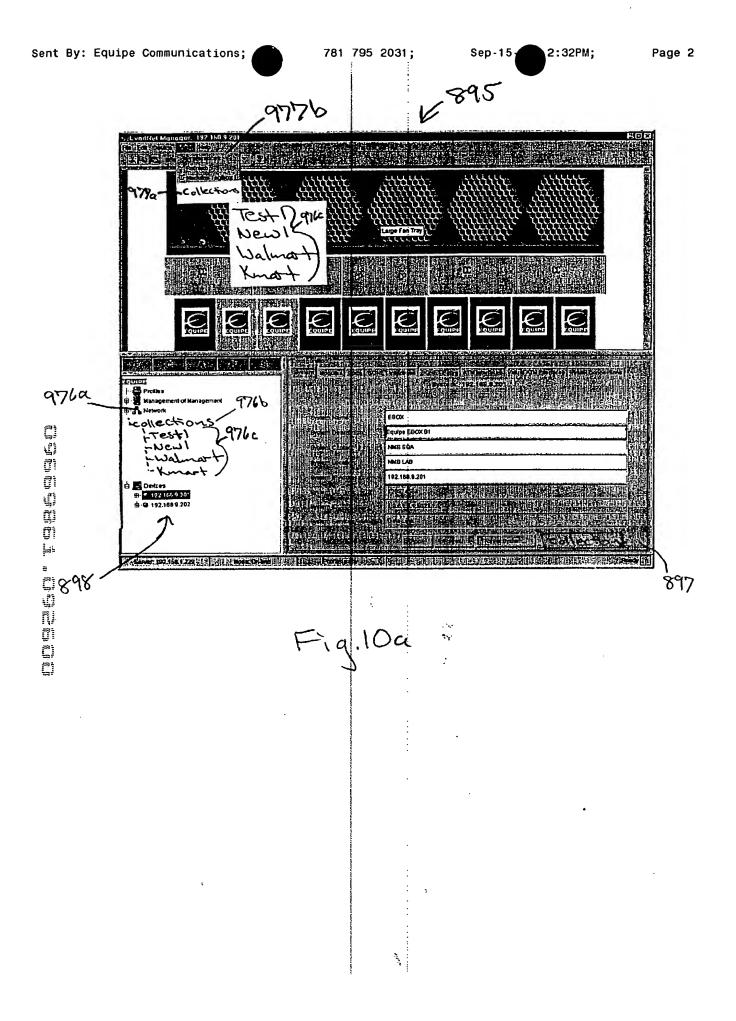












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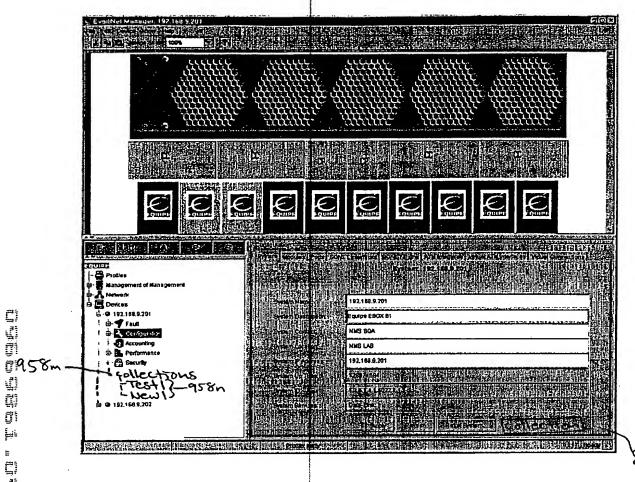


Fig. 106

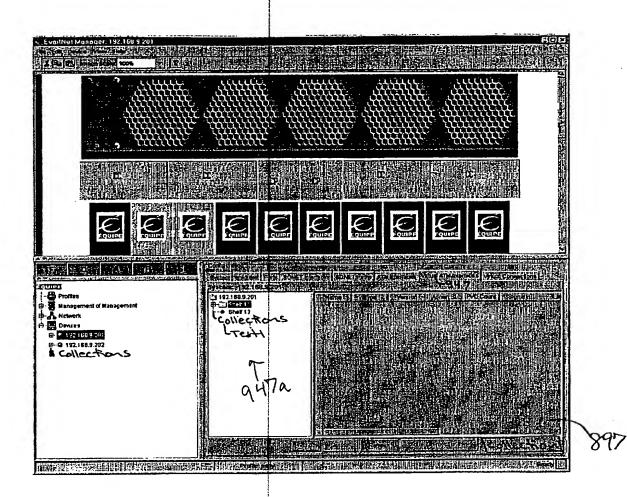
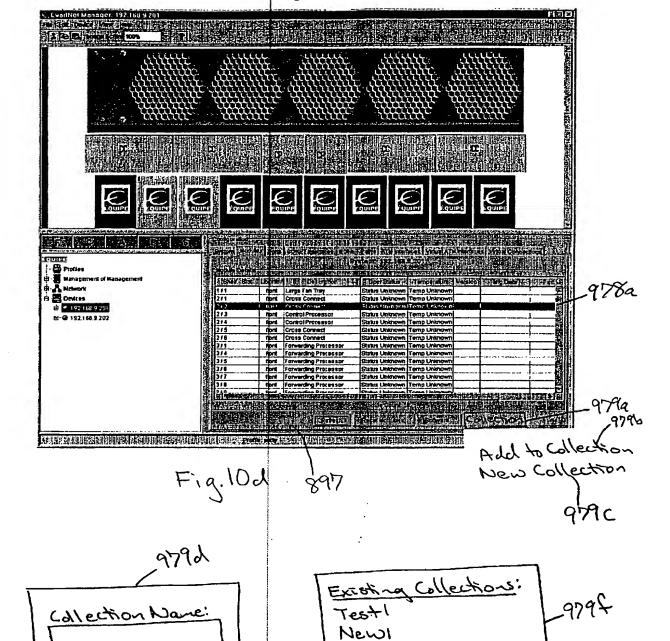


Fig. 100

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Fig. 10e

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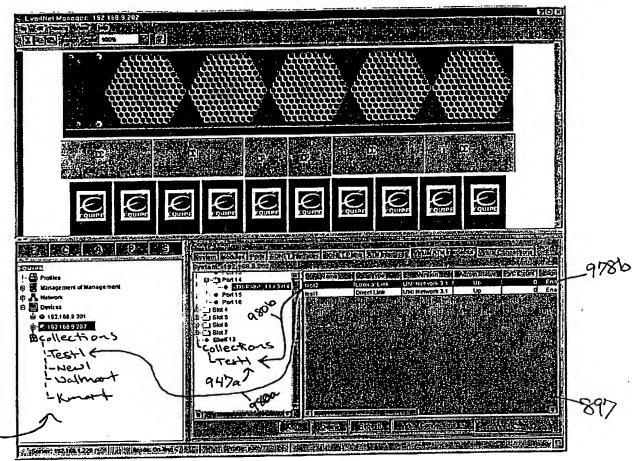


Fig. 109

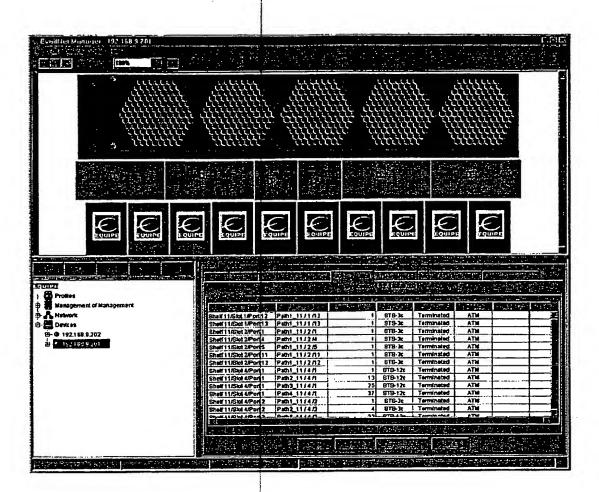


Fig. 10h

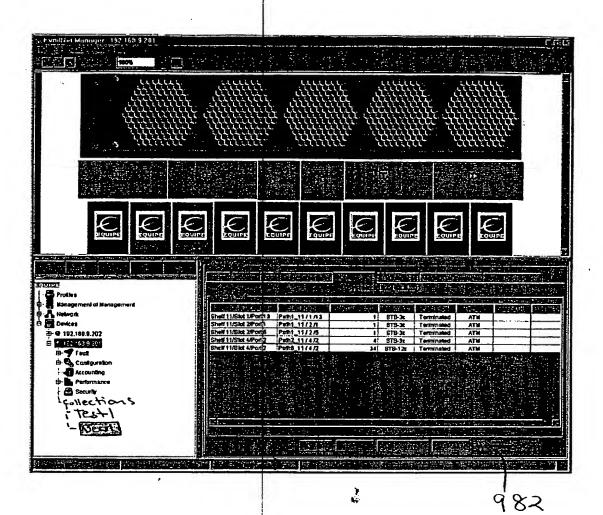
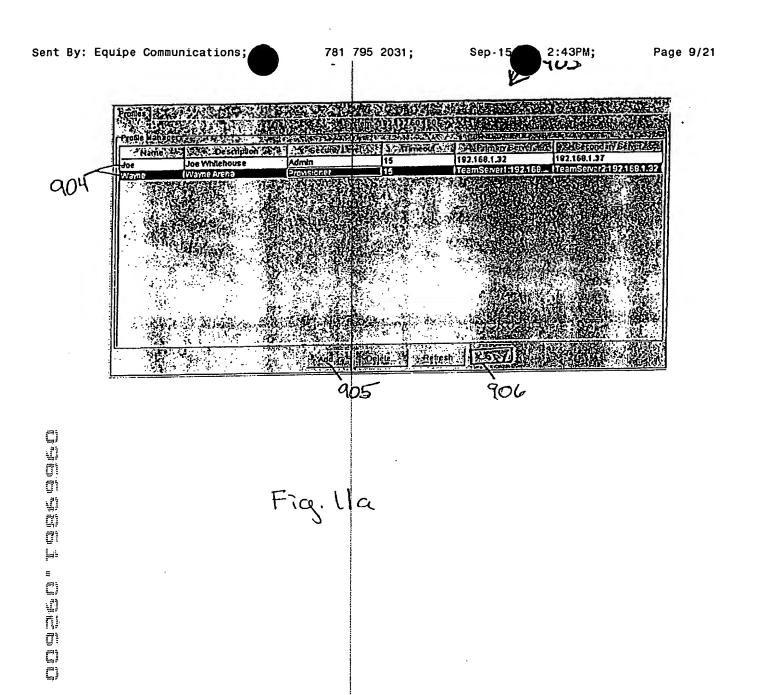
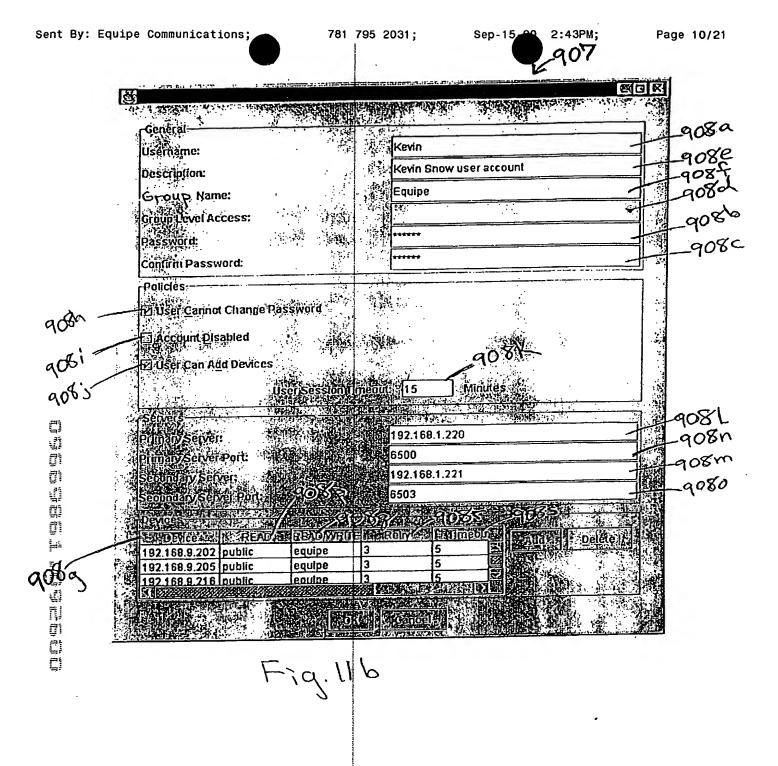


Fig. 10;



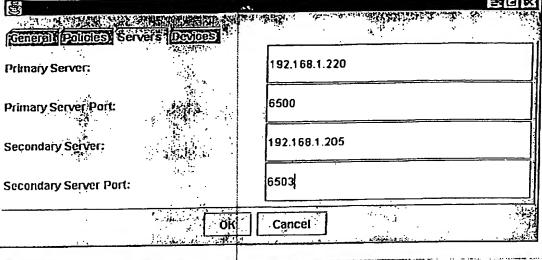


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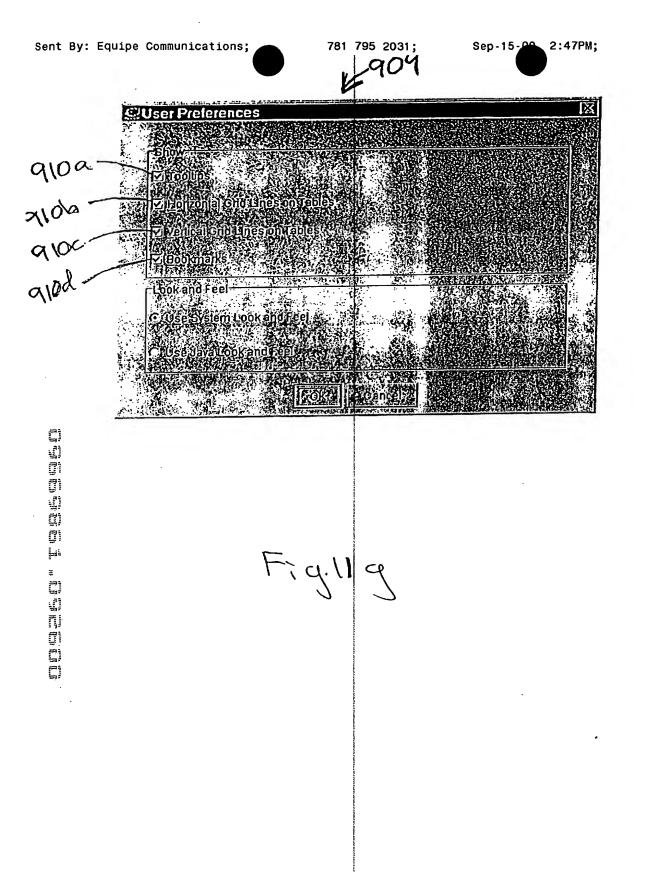
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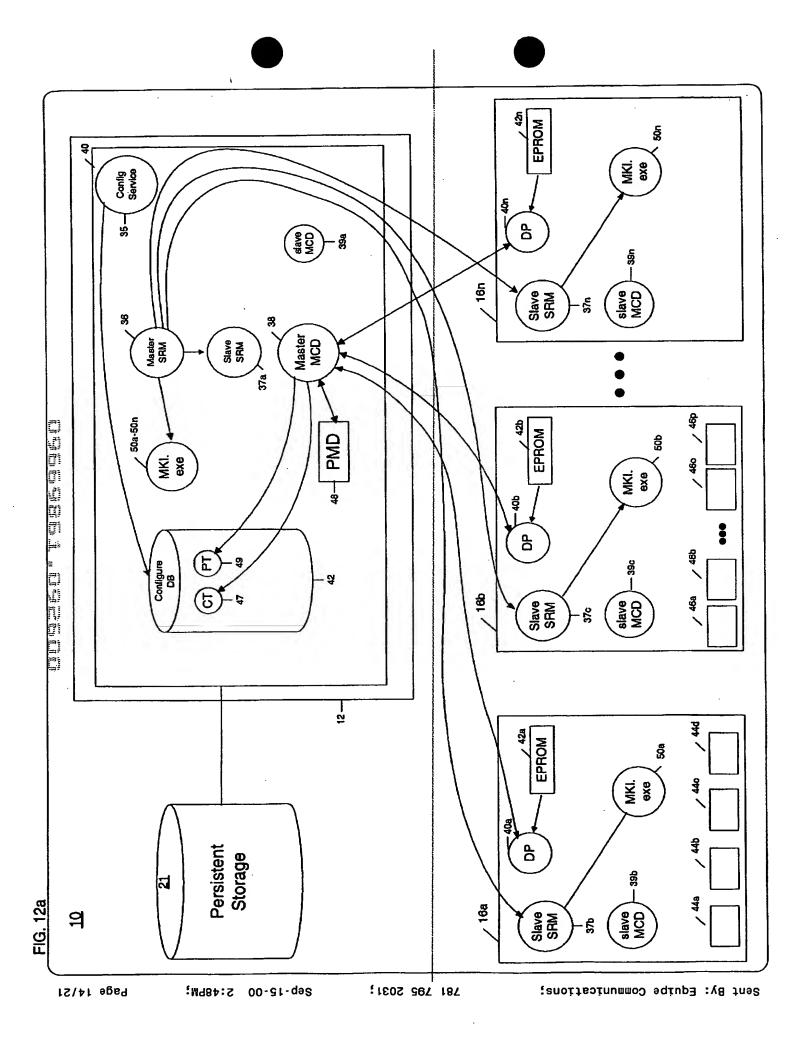


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Frg. 41f

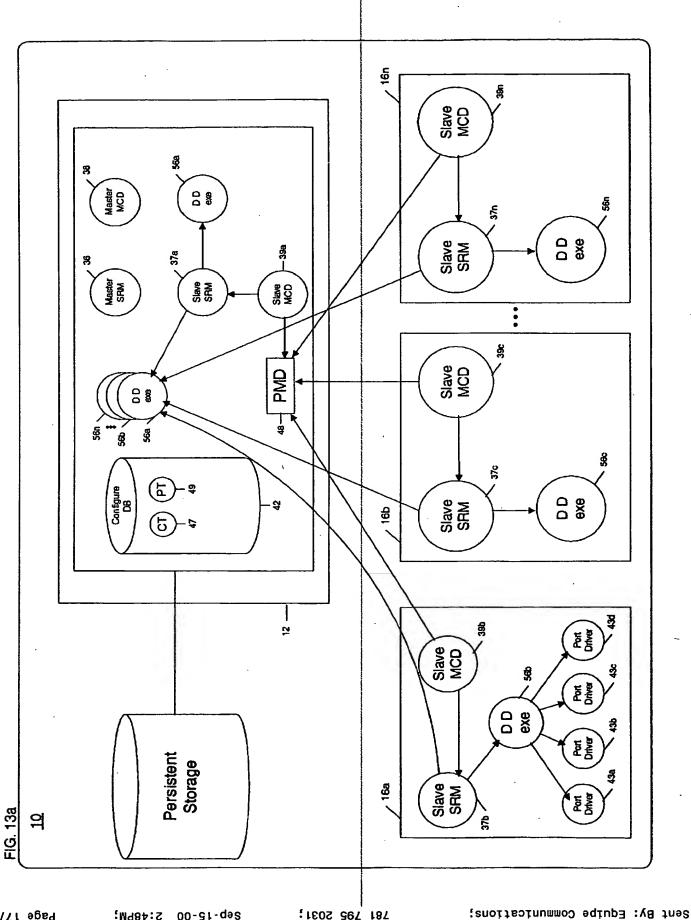


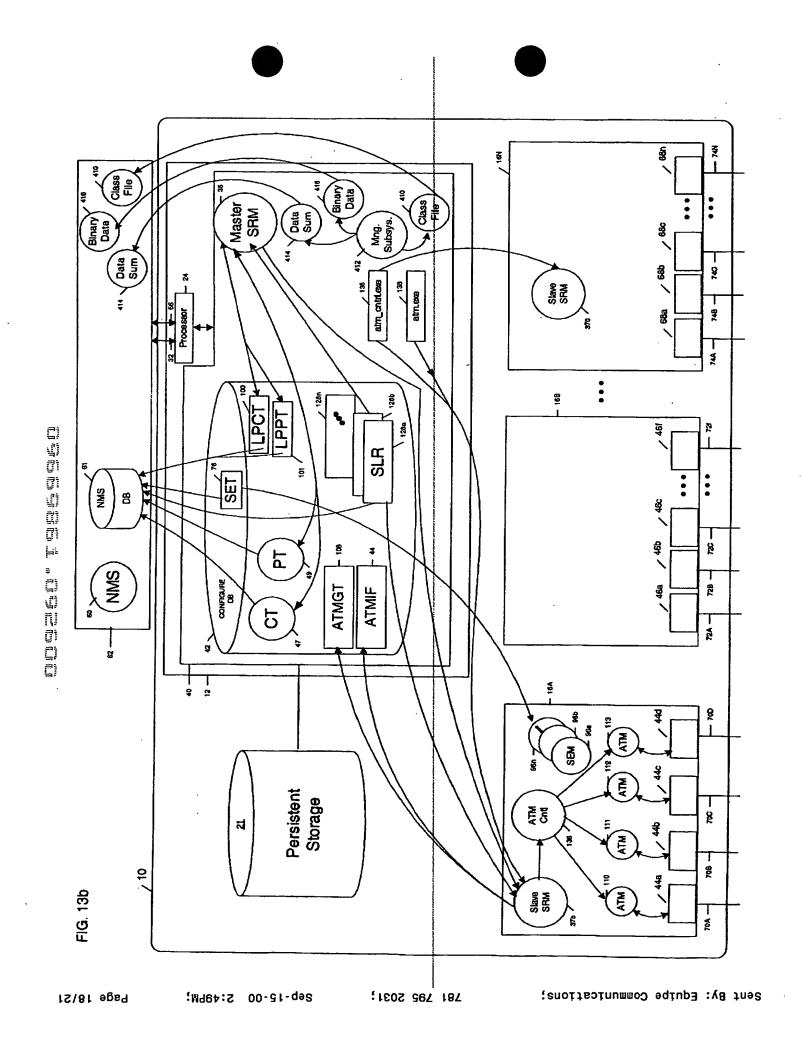
Page 13/21

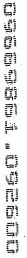


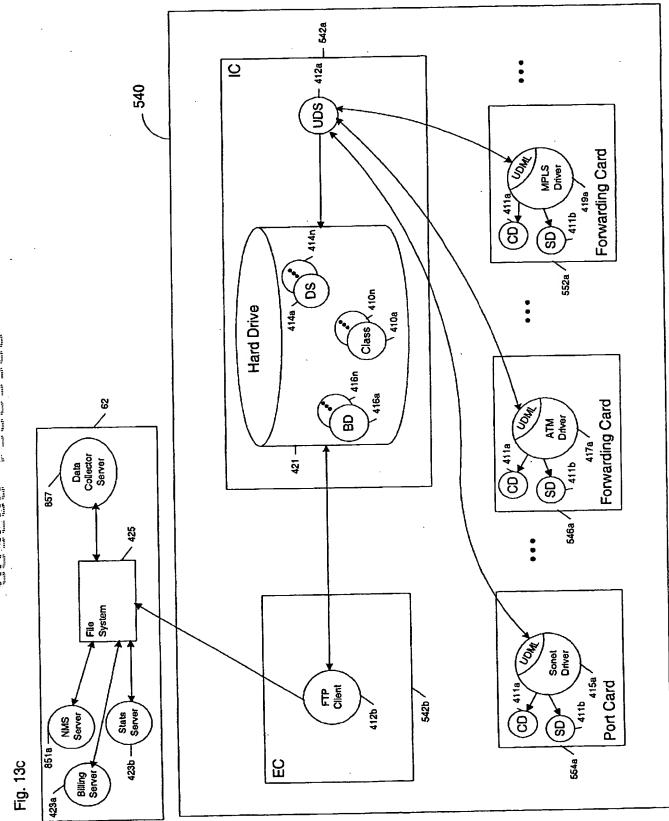
47	•			• • •		•	• •		•••
	SLOT NO.	-	2	•••	5	•	••.	12	•••
	VERSION SLOT NO. NO.	က	4	•••	1	•	• •	-	•••
	CWD TYPE	0XF002	0XF002	• • •	0X6002	•	• •	0XF002	•••
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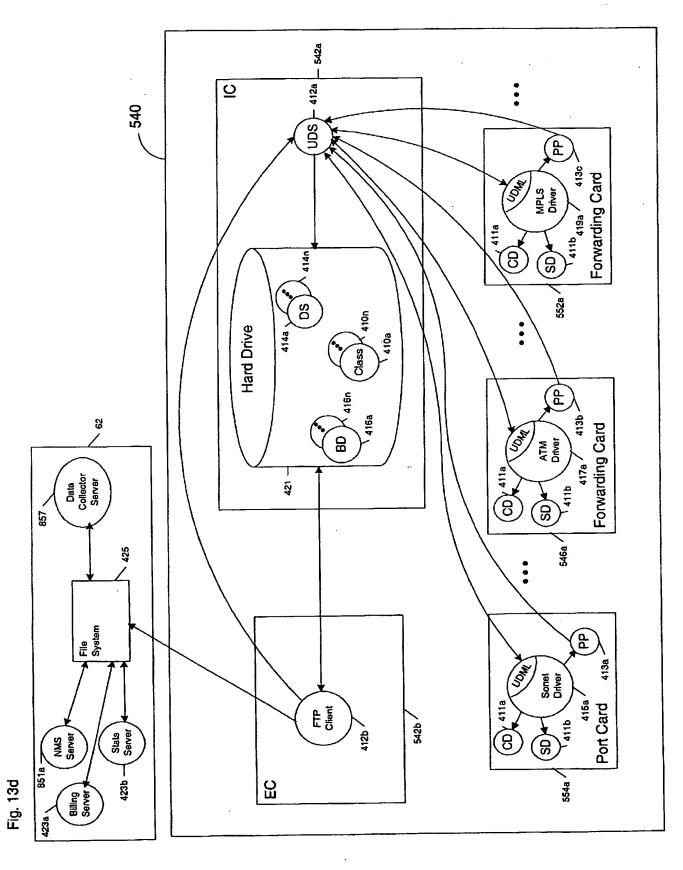


FIG. 14a

Service Endpoint Table 76

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	Servio Endpoi		Port PID
78	1		1500
80	2		1501
82	3		1501
84	4		1501
86	5		1502
88	6		1502
90	7		1503
92 —	8		1503
94 —	9		1503
168	10		1502
	:		
		Ł	

FIG. 14b

Logical to Physical Card Table 100

Primary Back-	04
	ъ
LID PID PID	
106 30 500 513	\Box
109 31 501 513	\Box

FIG. 14c

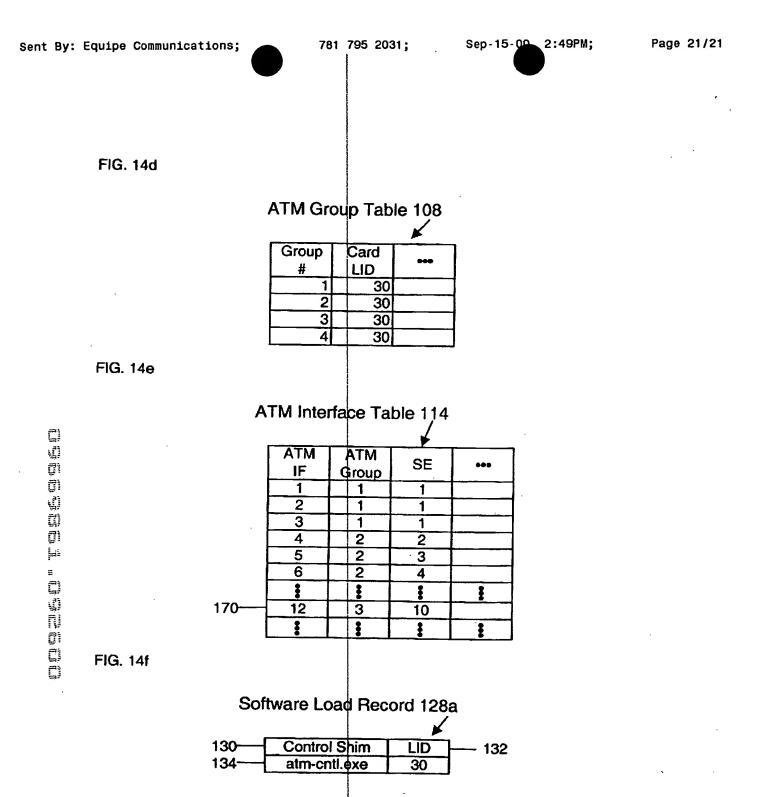
Logical to Physical Port Table 101

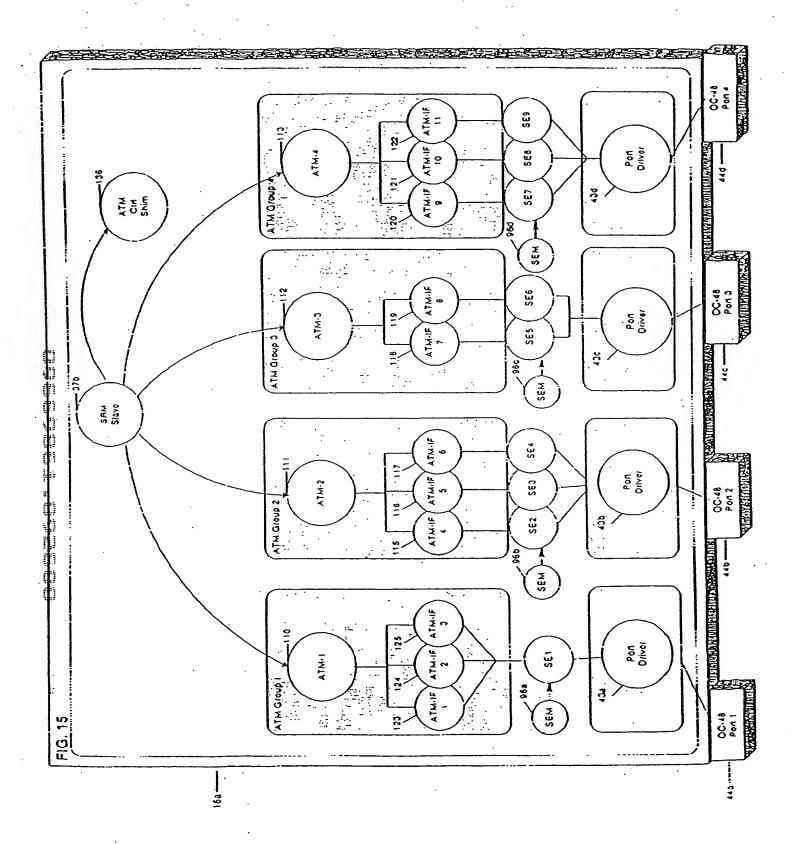
98 102 104

Primary Back-up

LID PID PID

107 40 1500 1600





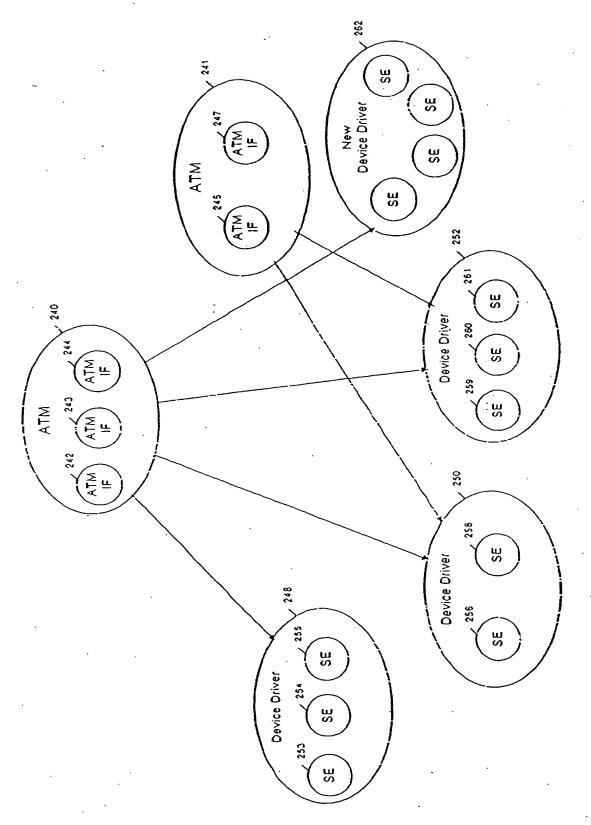
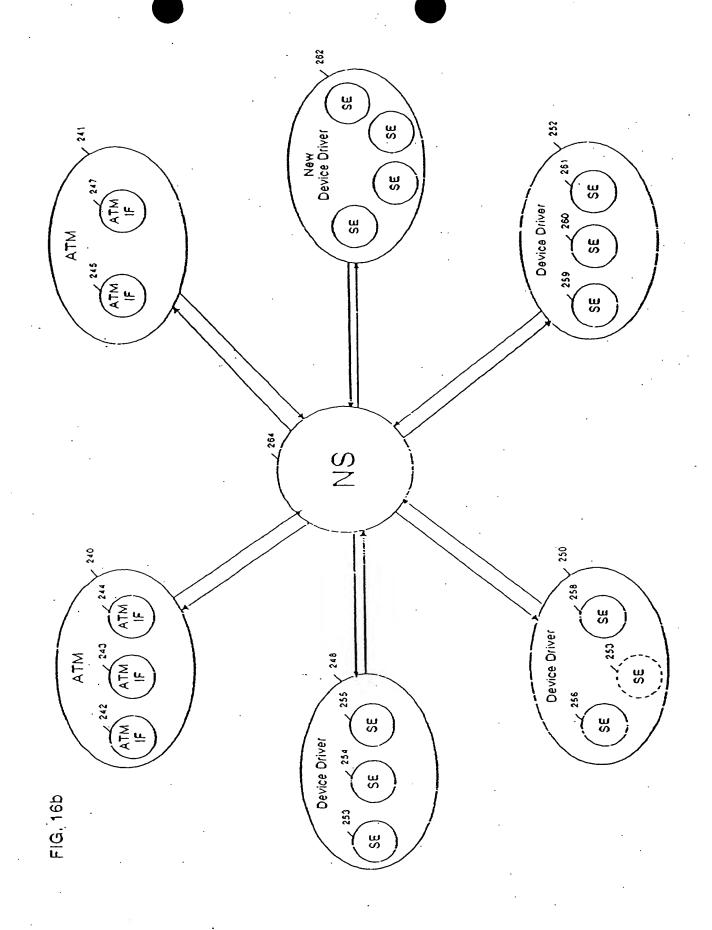
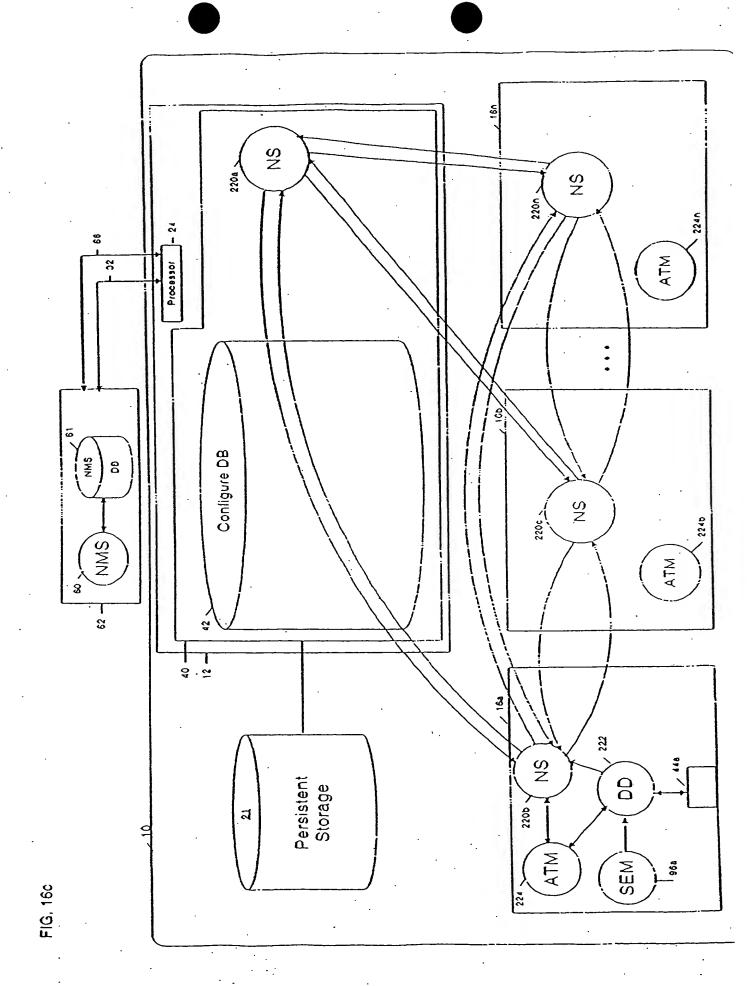
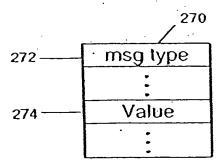
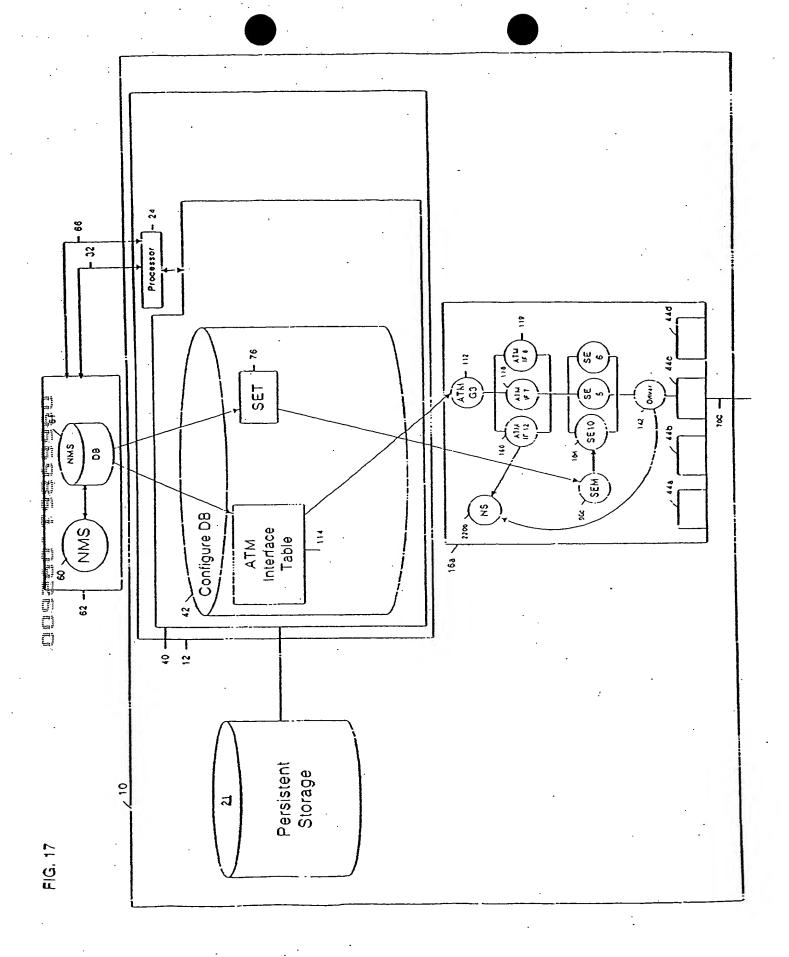


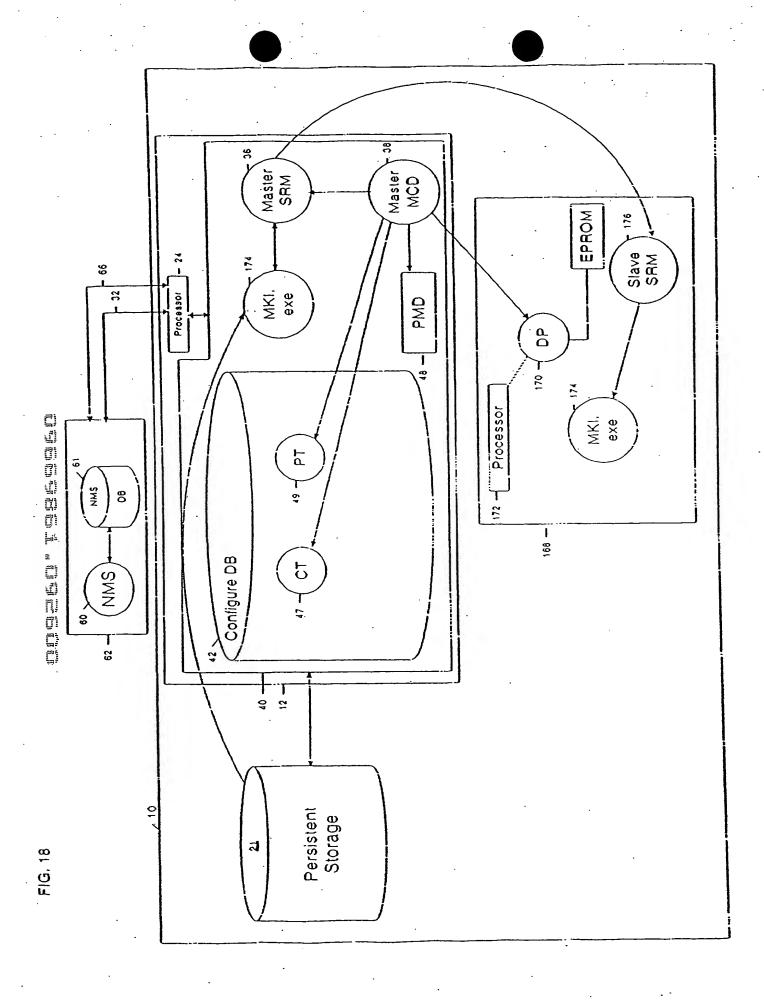
FIG. 16a

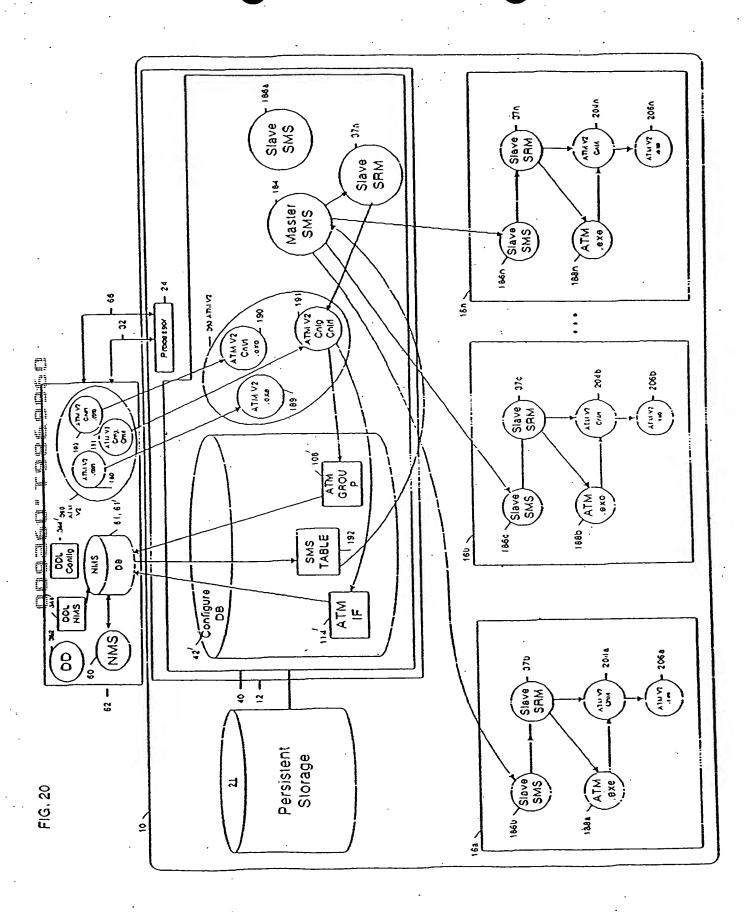


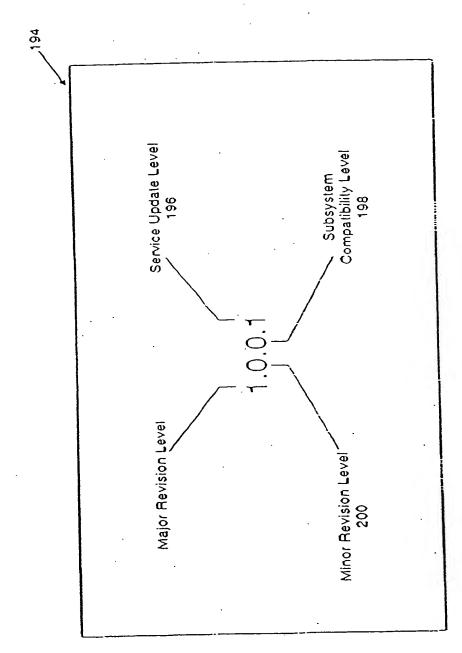












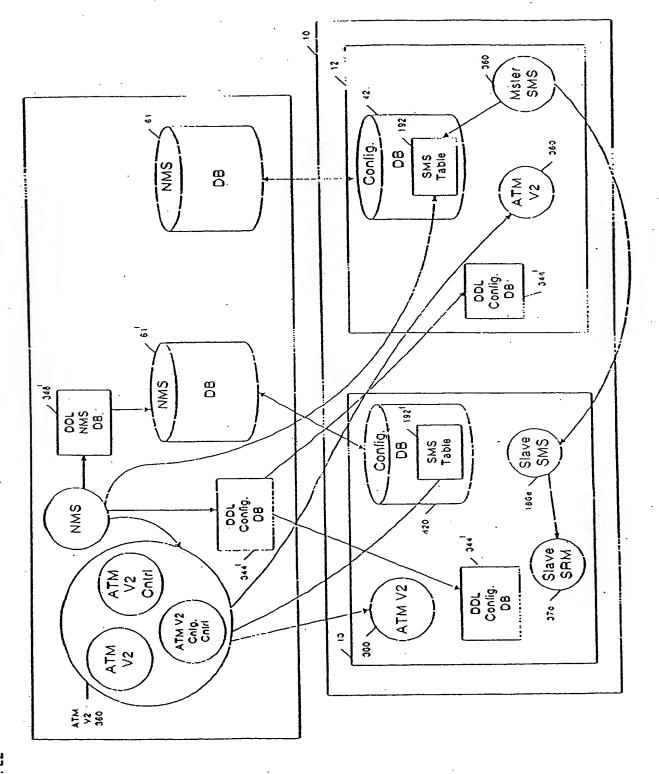
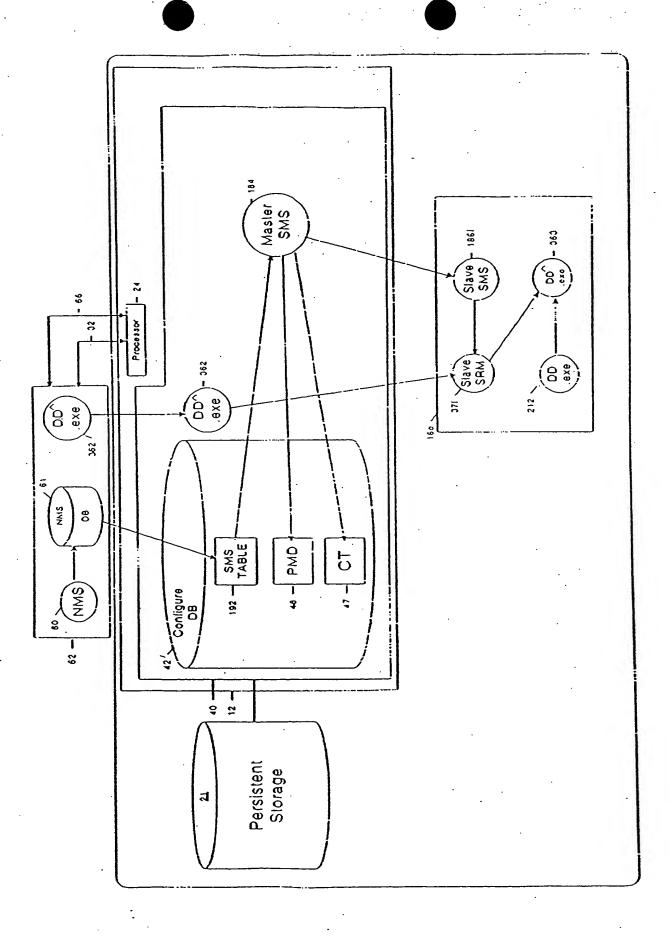
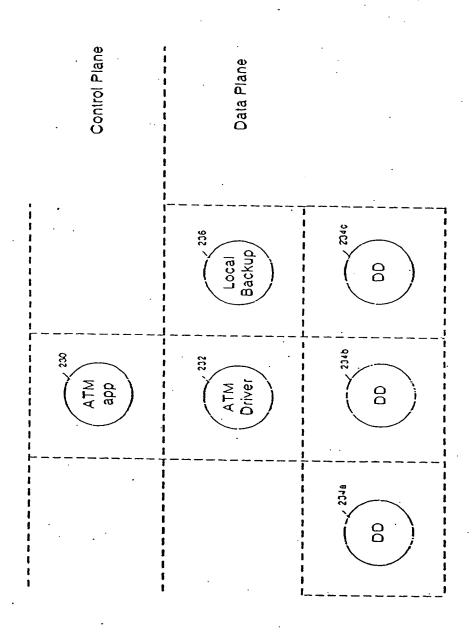
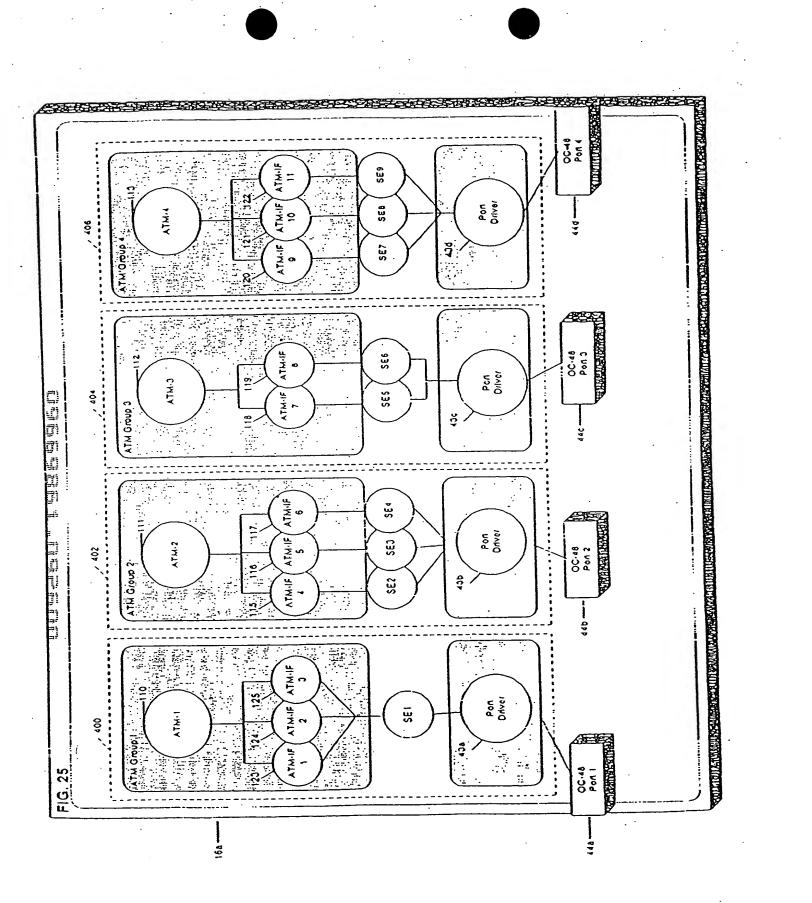


FIG. 22







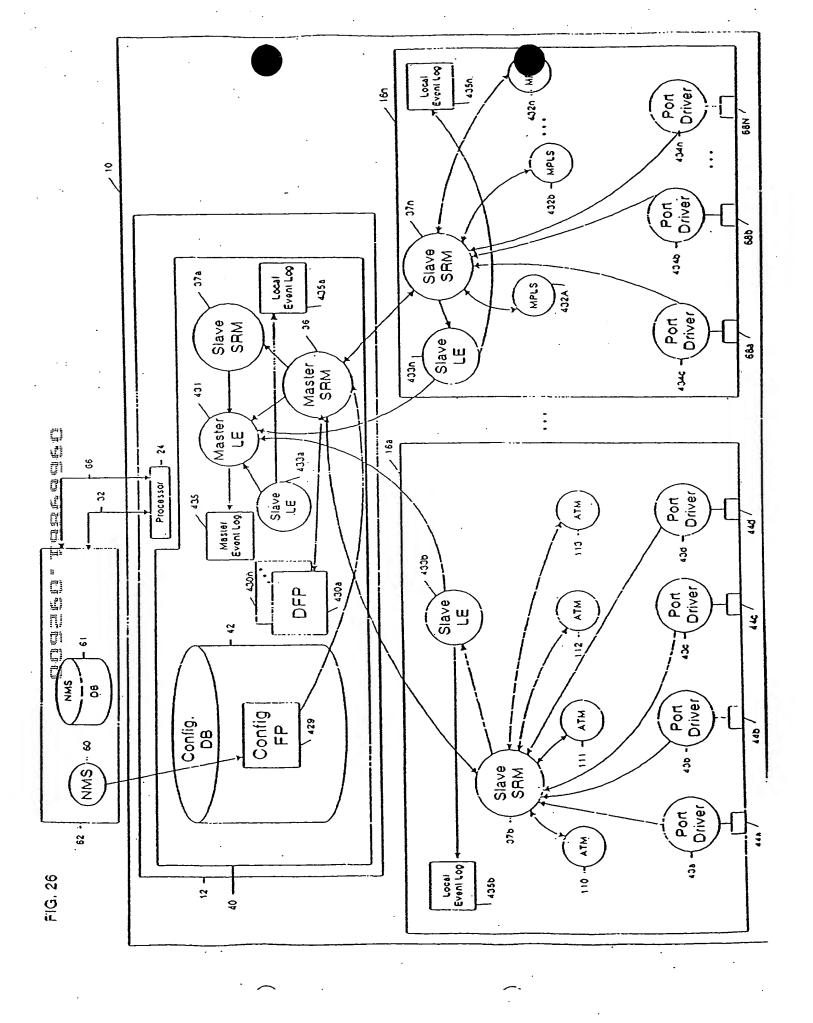
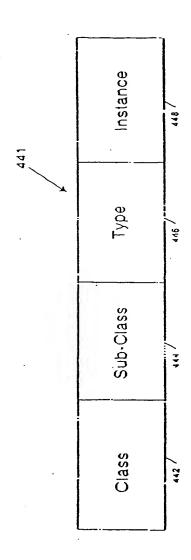


FIG. 27



Group Primary Card LID Card LI	
# Card LID Card LID 450 — 1 30 31 451 — 2 30 31 452 — 3 30 31 453 — 4 30 31 454 — 5 31 32	
# Card LID Card LID 450 — 1 30 31 451 — 2 30 31 452 — 3 30 31 453 — 4 30 31 454 — 5 31 32	
# Card LID LID 450 — 1 30 31 451 — 2 30 31 452 — 3 30 31 453 — 4 30 31 454 — 5 31 32	
450 — 1 30 31 451 — 2 30 31 452 — 3 30 31 453 — 4 30 31 454 — 5 31 32	
452 — 3 30 31 453 — 4 30 31 454 — 5 31 32	
453 — 4 30 31 454 — 5 31 32	
454 — 5 31 32	
	\neg
455 — 6 31 32	
456 — 7 31 32	\neg
457 — 8 31 32	
458 — 9 32 30	\neg
459 — 10 32 30	\neg
460 — 11 32 30	\exists
461 — 12 32 30	

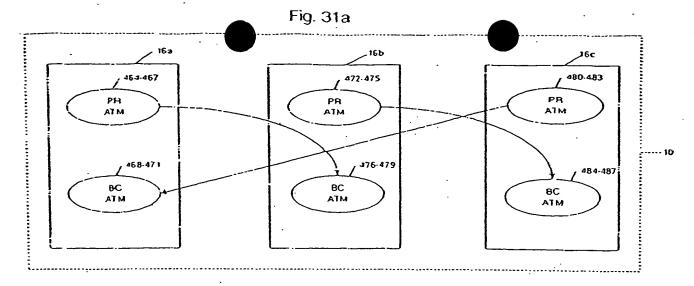
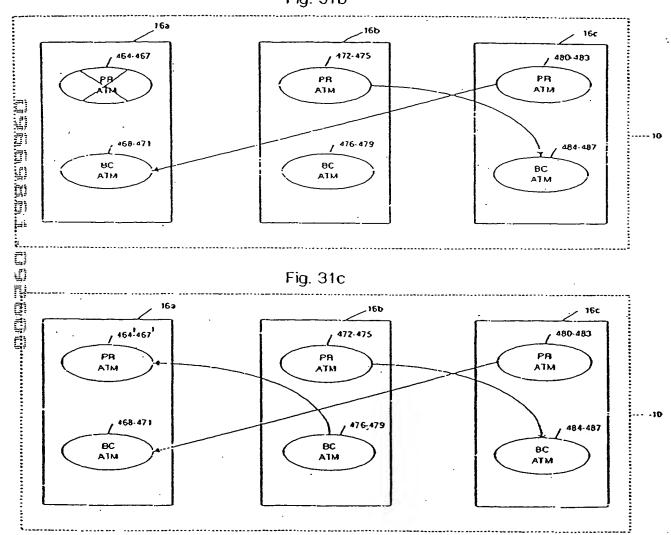


Fig. 31b



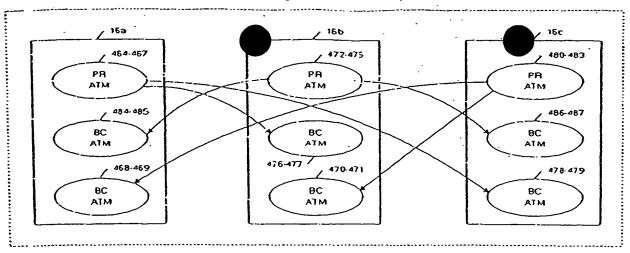
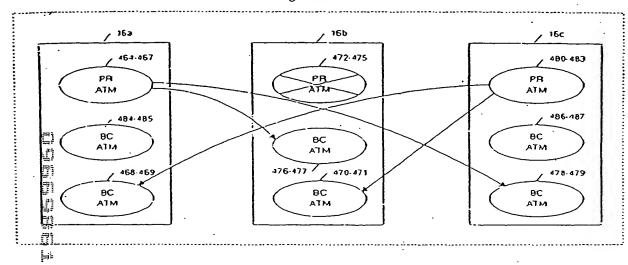
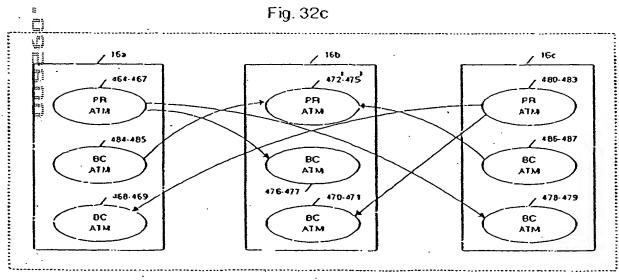
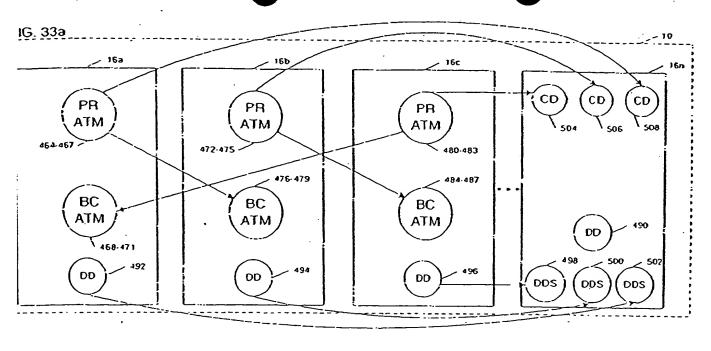
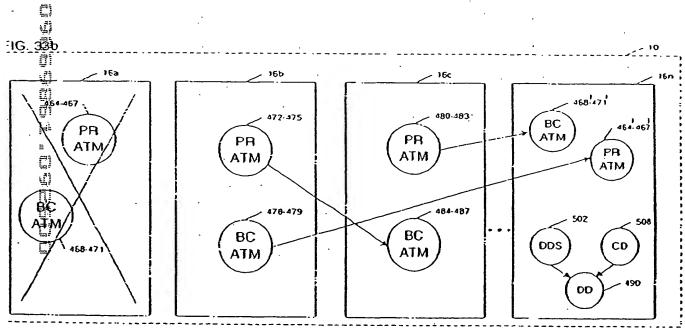


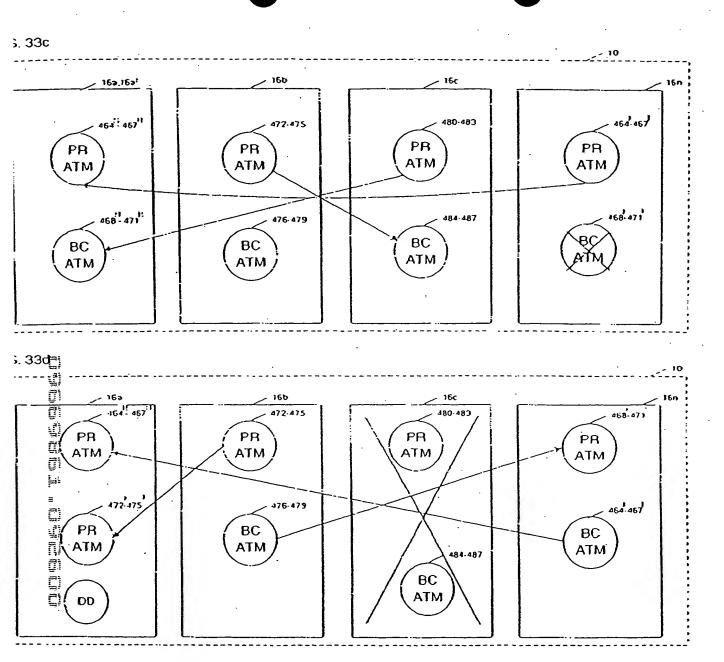
Fig. 32b

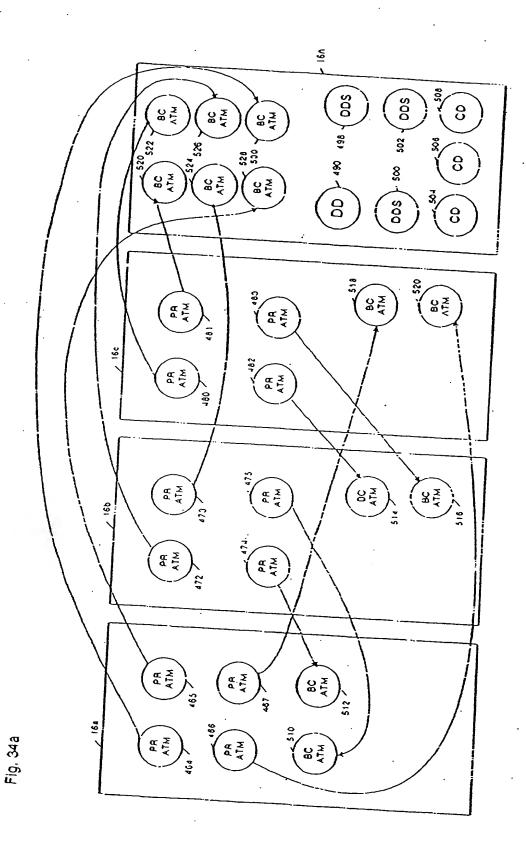


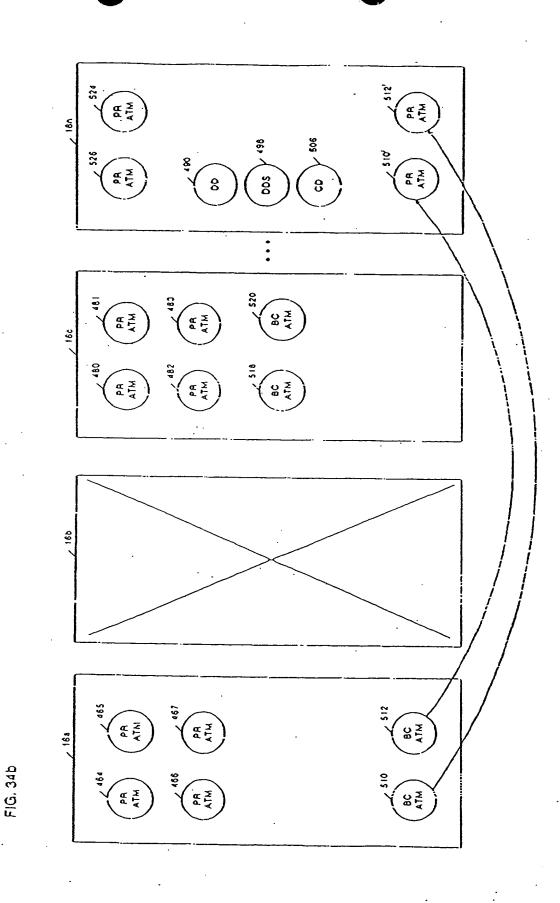




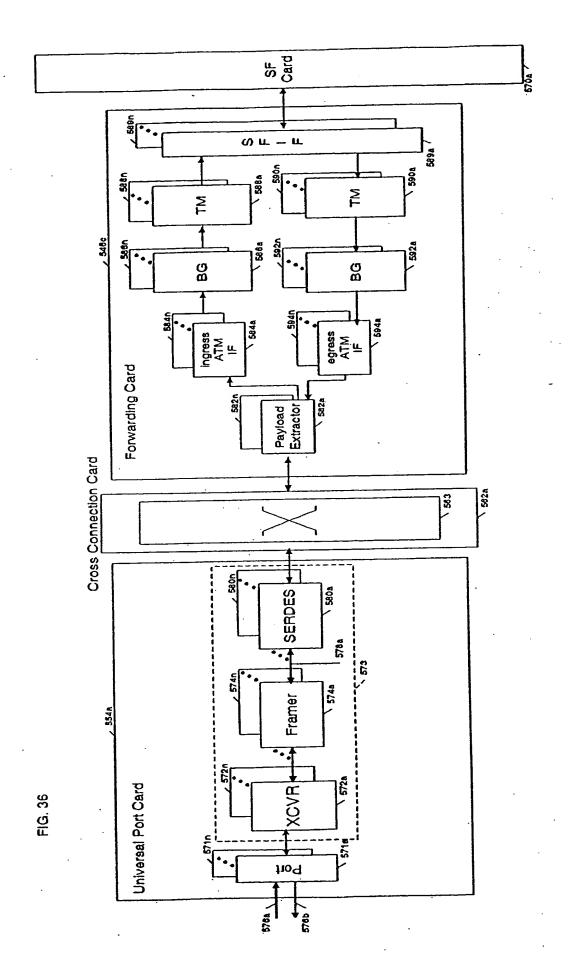








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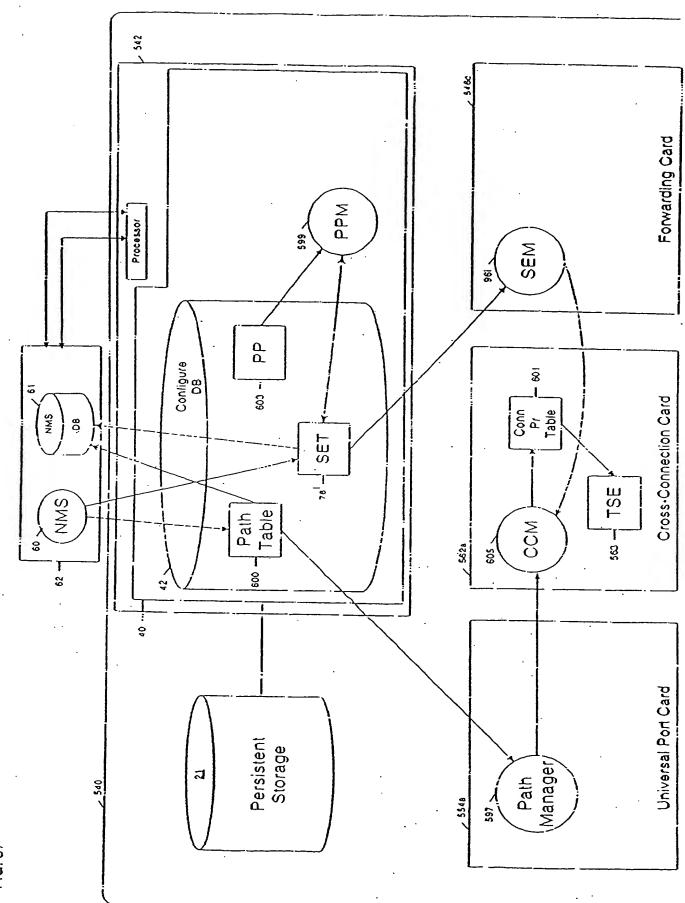


FIG. 37

Path Table 600

		• • •
# of Time Slots	3	• • •
Time Slot	4	
UP Pon LID	1231	•••
Path	1666	•••
	602	

FIG. 39

				• • •
Service End Point Table 76'	610	Path PID	1666	• • •
	× 809	FC Time Slot		• • •
	909	FC Slice		
se End		FC LID		•.••
Servic		O #	-	• • •
	-	S #	878	• • •
			604	

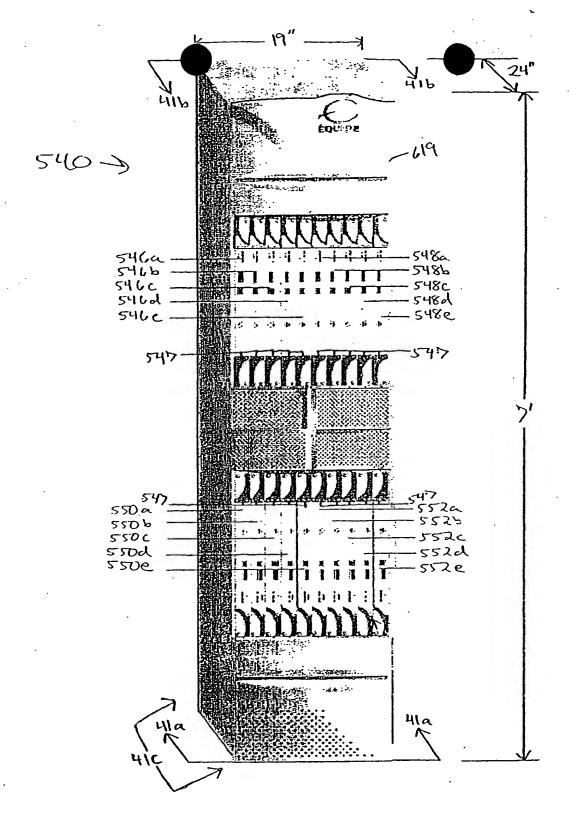


Fig. 40

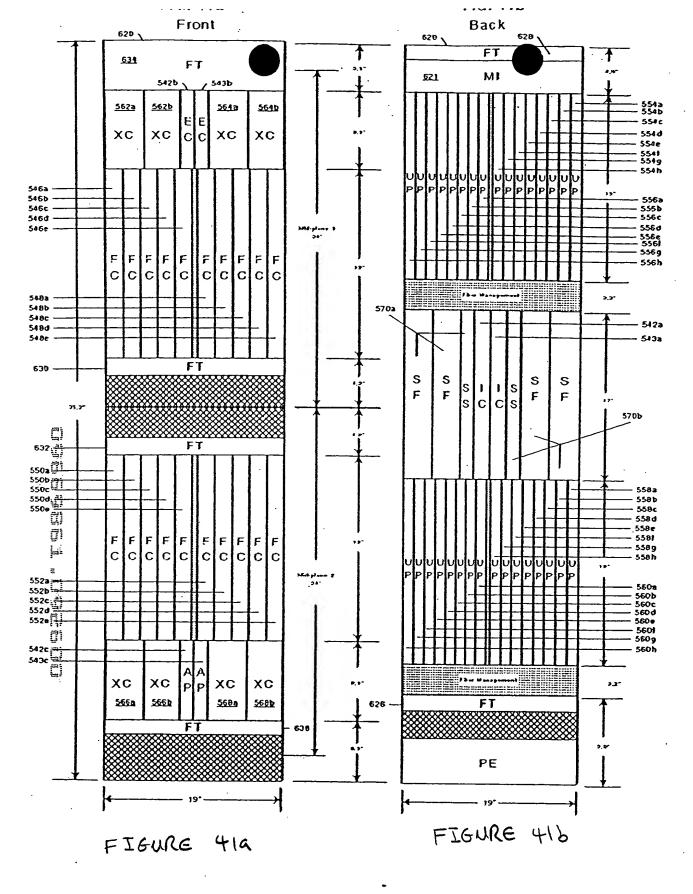


FIGURE 41C

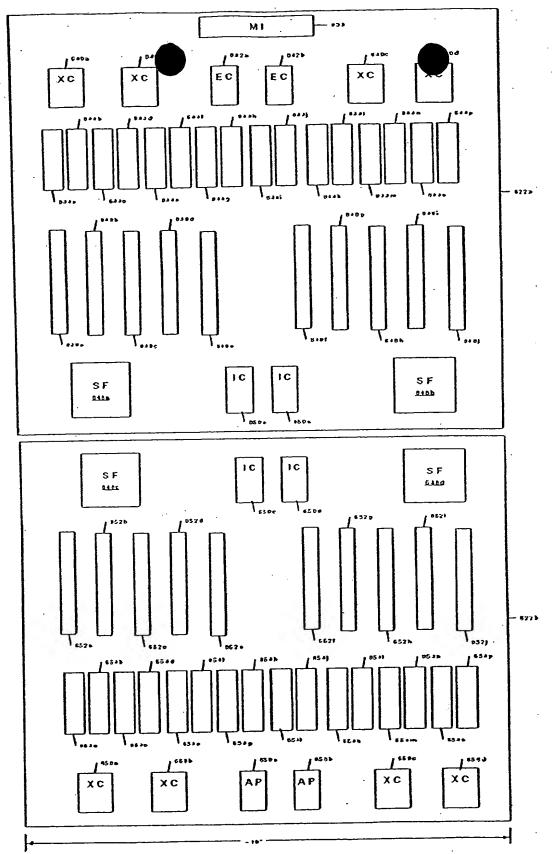
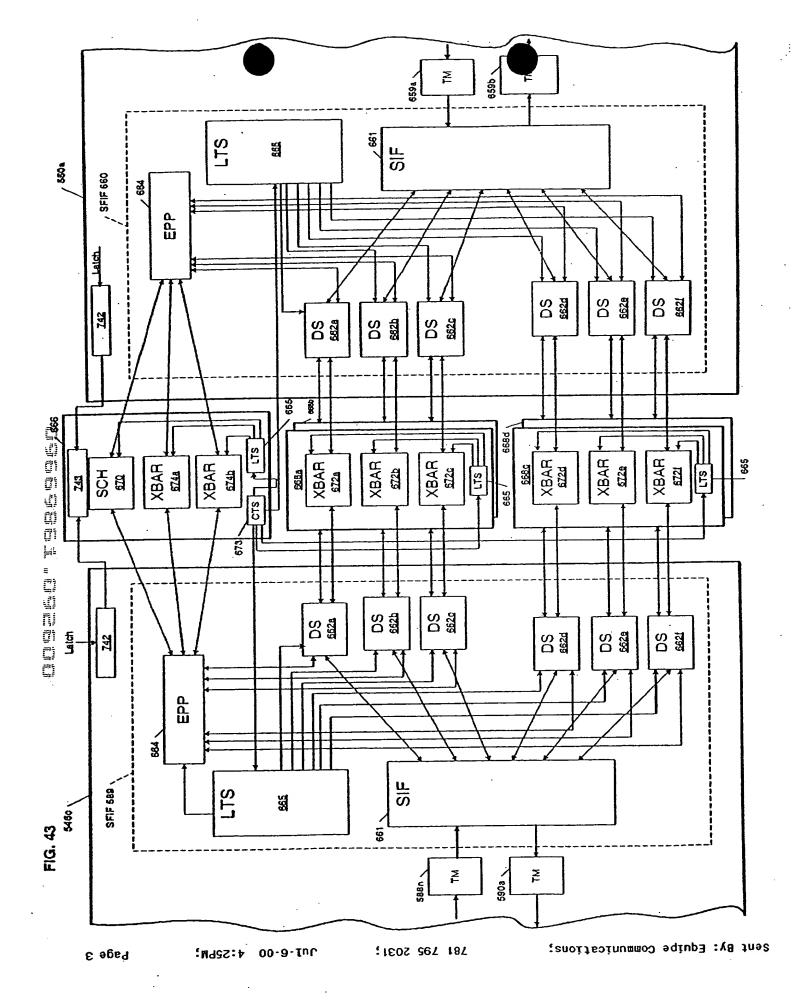
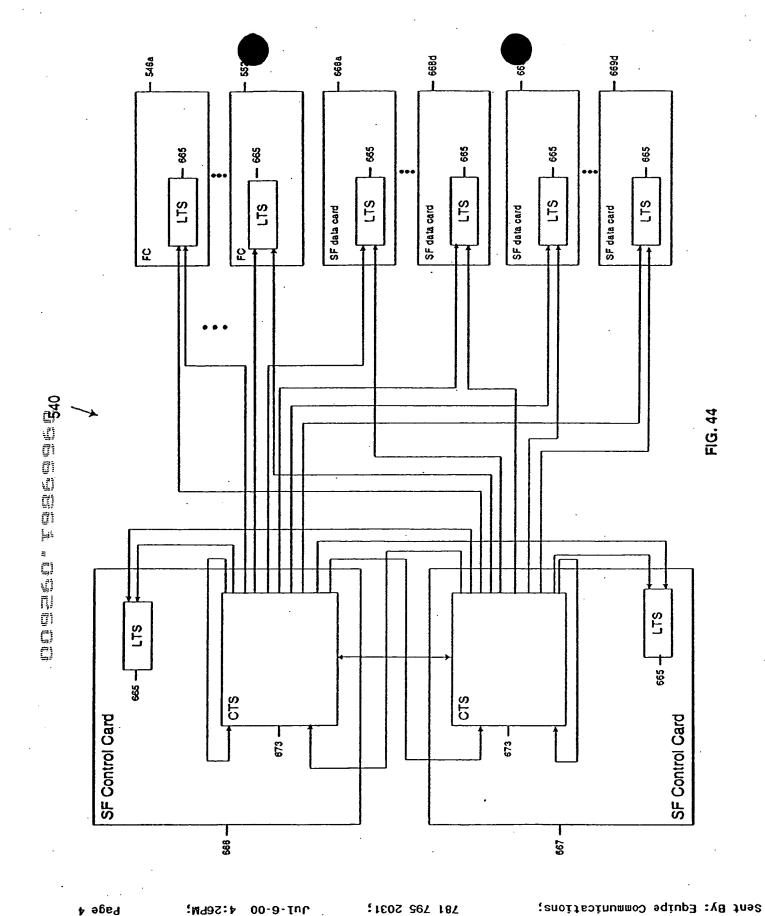


FIGURE 42





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Page 4

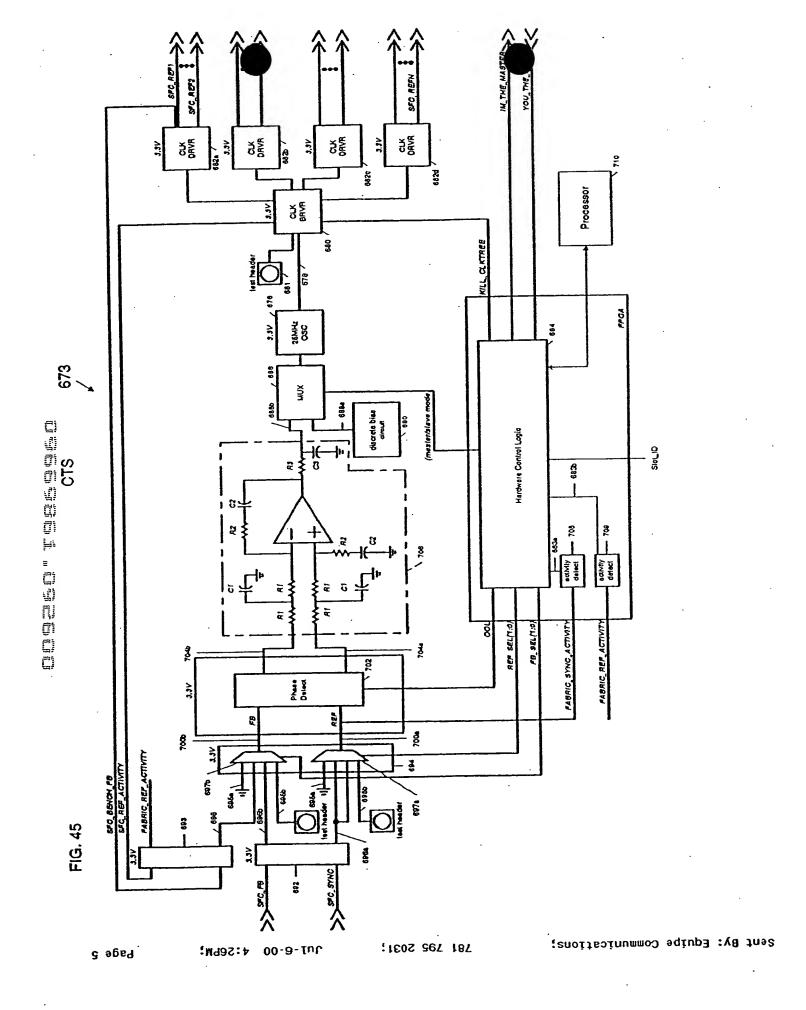
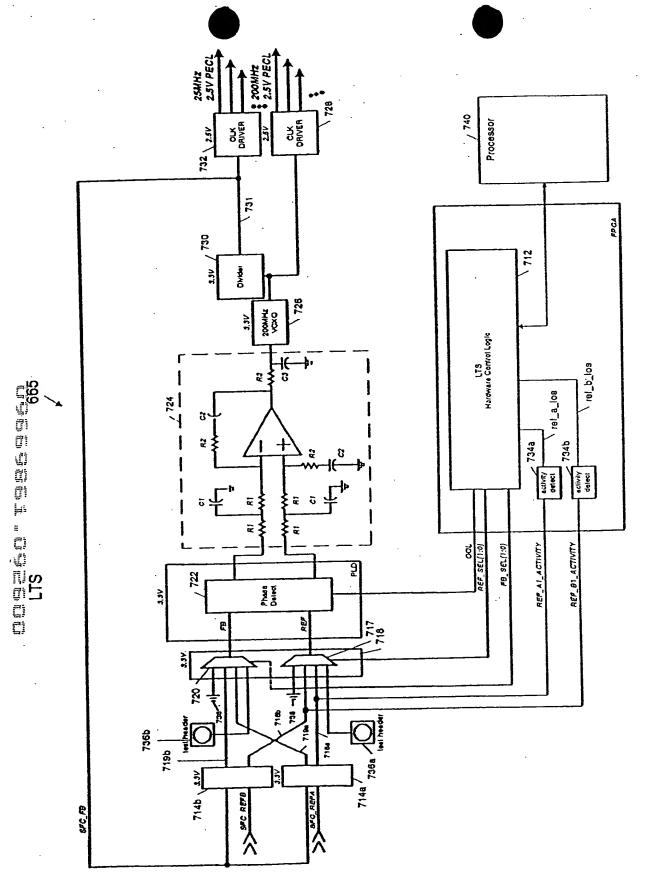


FIG. 46





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Page 7

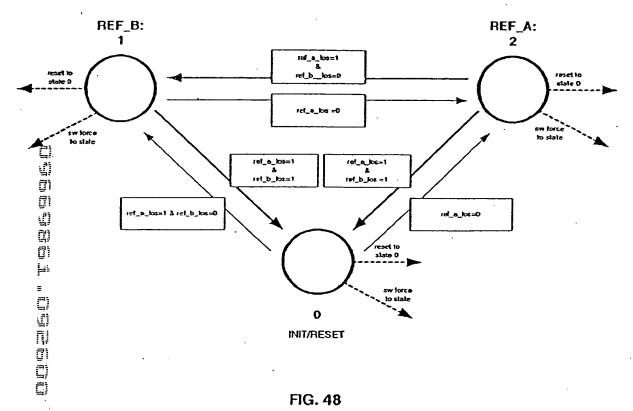
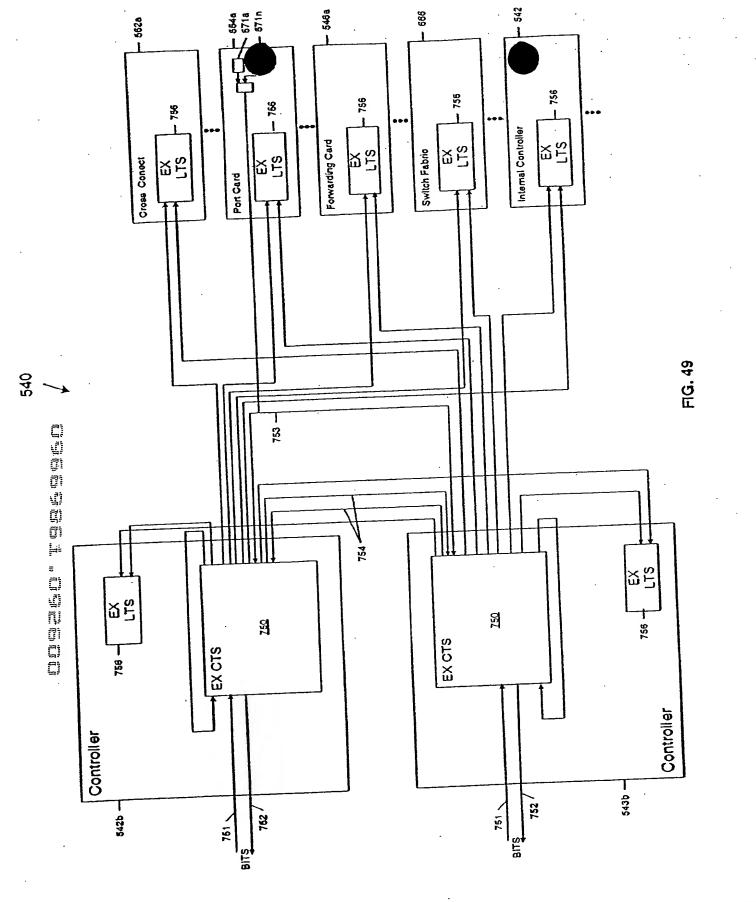
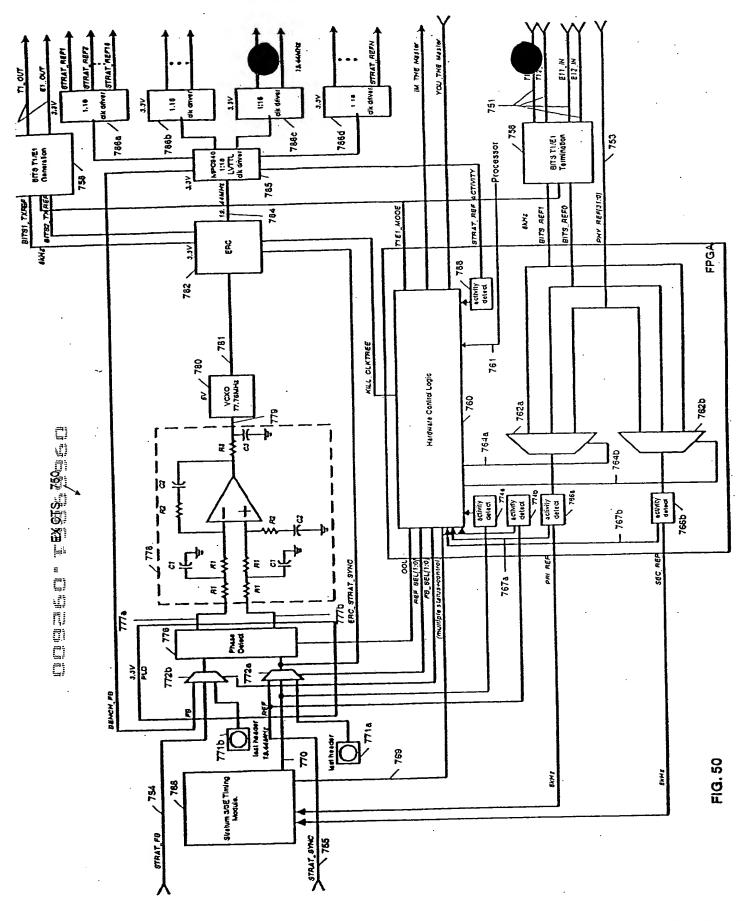


FIG. 48



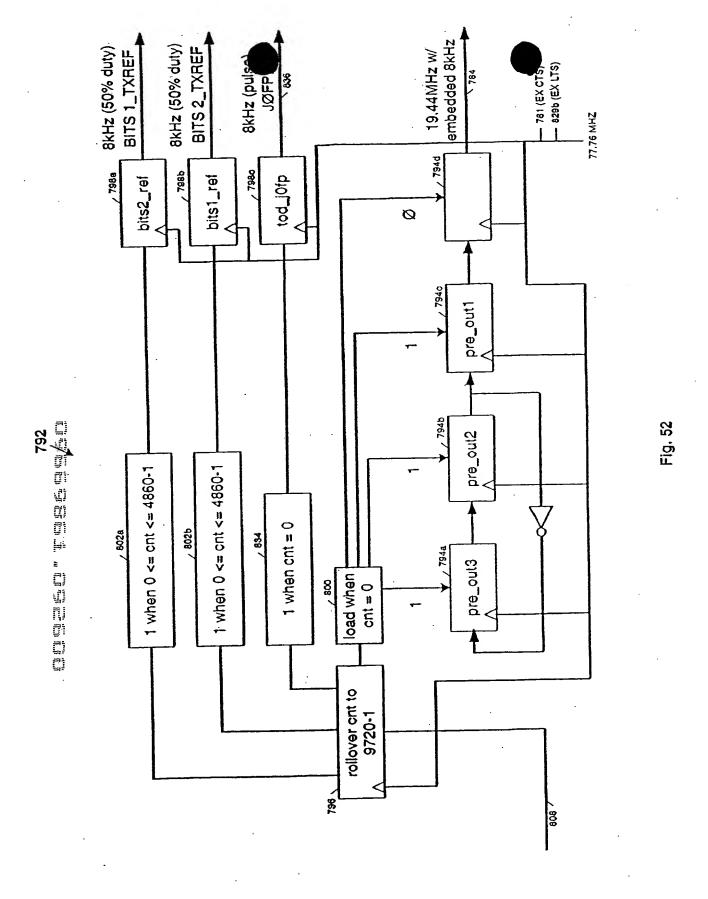
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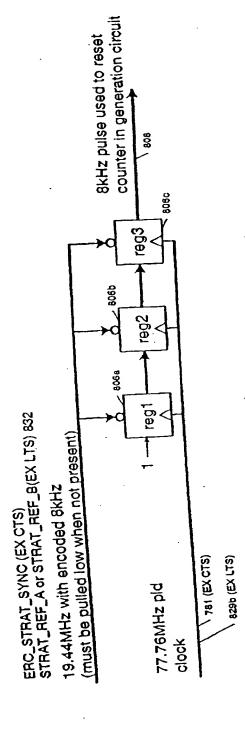
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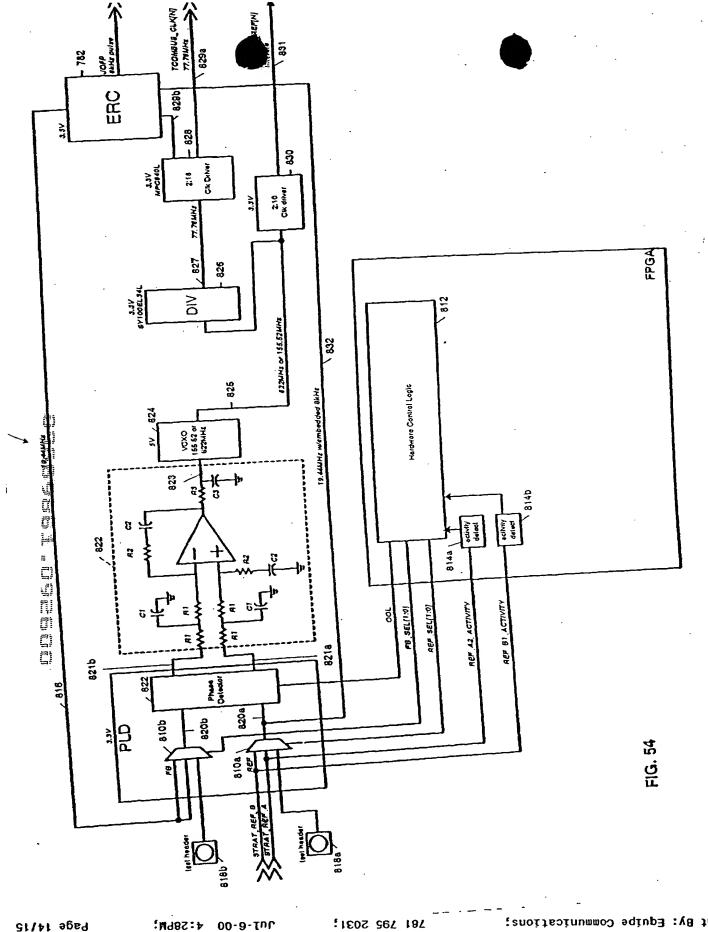


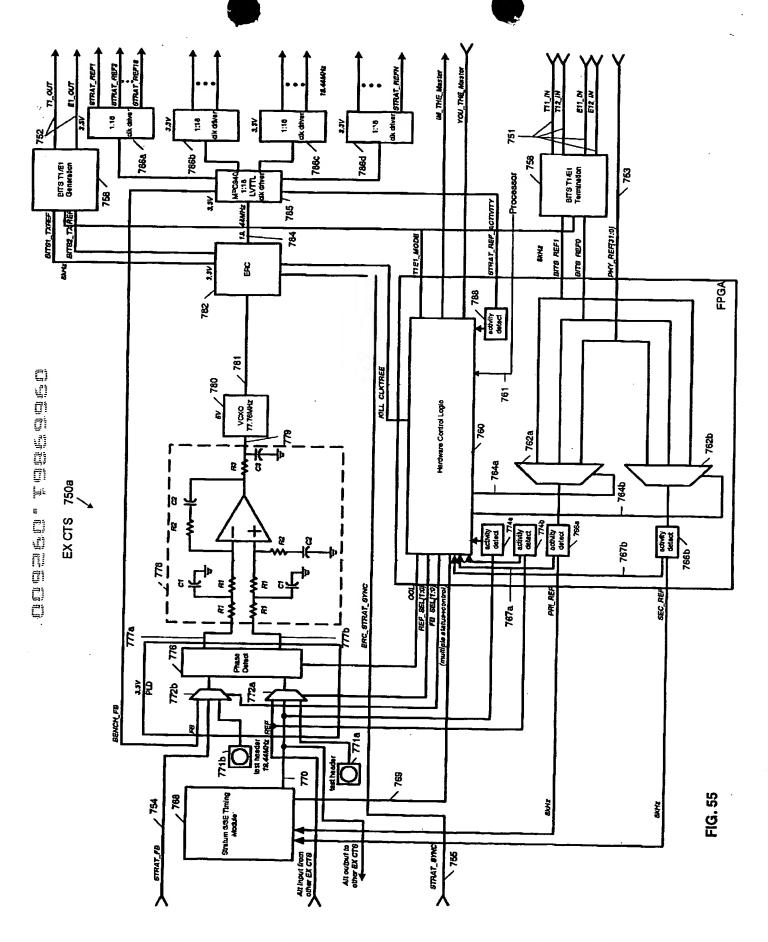
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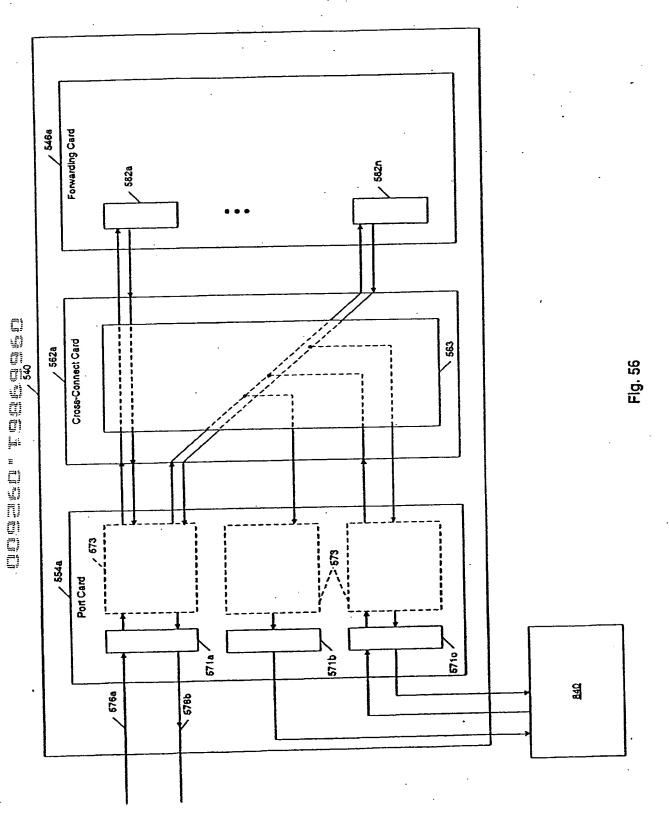


Extractor FIG. 53

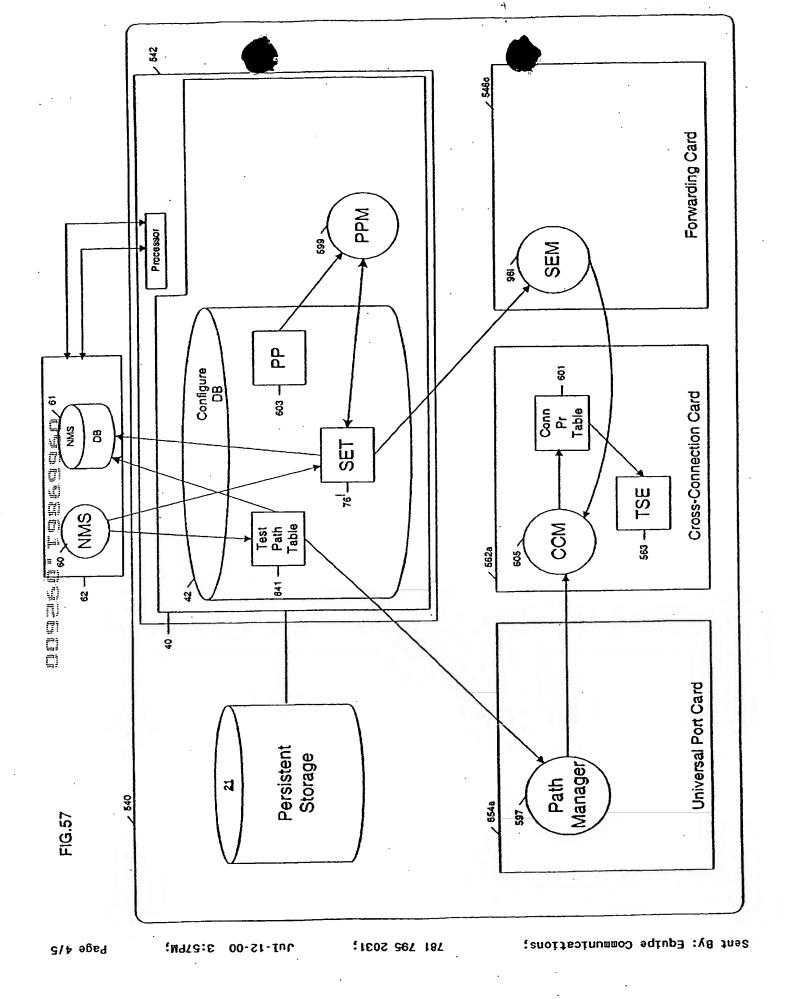




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	845	Enable	Port	Receiver	No	No	Yes		
Test Path Table 841	844		Monitor		Ingress	Egress	Ingress		_
st Path		# of	Time	Slots	က	က	က	•	• •
₽ ×			Time Slot		4	4	4	•	• •
·		QD.	Port	2	1232	1233	1233		• •
	•	4	רומך היה	3	1666	1666	1666		• (
	·				842	843	844	-	

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